多利吉科技
CoreSolid Storage

Industrial CompactFlash™ Card

Gaia HAK40 Series

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Revision	Date	Major Changes
A.0	2009/3/13	1. Add product picture in top page 2. Revise notice in section 2.6. 3. Revise section 8 **Contact Information**
A.1	2009/09/17	1. Modify minimum capacity from 1GB to 128MB in section 2.2.3 Capacity and Block Size information. 2. Update to Global Wear-Leveling in section 2.3.4 Wear Leveling. 3. Update Testing Conditions: 75cm height in section 2.4.3. Bare Drop Testing. 4. Update Sine Vibration 15Grms in section 2.4.4 Vibration. 5. Revise 2.5.3 MTTF (Mean Time To Failure) 6. Update Installation picture in section 5.2 Partition.

1. Product Description

1.1 Product Overview

HAK40 series is Industrial CompactFlash Storage Card based on FLASH memory controller technology. This card complies with CompactFlash specification. It is suitable for the usage of data storage memory for Industrial PC or other electric equipments. This card is equipped with NAND FLASH memory. By using this card it is possible to operate stability for the systems that have CompactFlash slots.

HAK40 series support Fixed or Removable mode. Setting to fixed mode can be used in systems for some operating system that can not accept boot-up from Removable mode disk like Windows XP. With this feature, HAK40 can support industrial PC or Thin client as the bootable device for the operation systems. Setting this card to Fixed or Removable mode will no any functional differences or issues during the operation.

HAK40 series provides SMART function that can allow the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action.

- ● **Application Fields:**
- ■ Industrial PC and Thin Client
- ■ Entertainment/Consumer Electronic Device
- ■ Game and Telecommunication Machine
- ■ Ticketing, Examining, testing machine
- ■ Army, Health and Production Equipment and Machine
- ■ Other machines and Equipments with CompactFlash™ Card Interface

1.2 Product Feature

- ■ CompactFlash™ specification 4.1 version compliant.
- ■ Following type I CompactFlash storage card dimensions.
- ■ PC Card ATA protocol compatible.
- ■ Support ATA SMART function.
- ■ Support PIO Mode 6, Multi word DMA mode 4, and Ultra DMA mode 4.
- ■ True IDE mode compatible.
- ■ High reliability with robust Error Correction.
- ■ Low power consumption.
- ■ Capable Operating as Boot Disk or Code Storage Device for Embeded Operating System
- ■ Data Storage Device with capacity up to 16GB.
- ■ Voltage 3.3V or 5.0V operation.

    Notice: *The performance will depend on different platform with different test result.*

1.3 System Requirement

The Host system which is connected to Industrial CompactFlash™ Storage Card should meet system requirements at minimum.

1.3.1 Power Requirement

■ Voltage: DC +3.3V ± 5% or DC +5.0V ± 10%

1.3.2 Operating System

● DOS
● Windows 98SE/ME/2000/XP/Vista
● WinXP Embedded/WinCE
● Linux

1.3.3 Interface

1. CFA4.1 compatible 50pin SMT connector and type I (3.3mm).

2. Specification

2.1 Physical Specification

2.1.1 Overlook

The overlook views of High Speed Industrial CompactFlash™ Storage Card are illustrated in Figure 1.

CompactFlash™ Card Connector
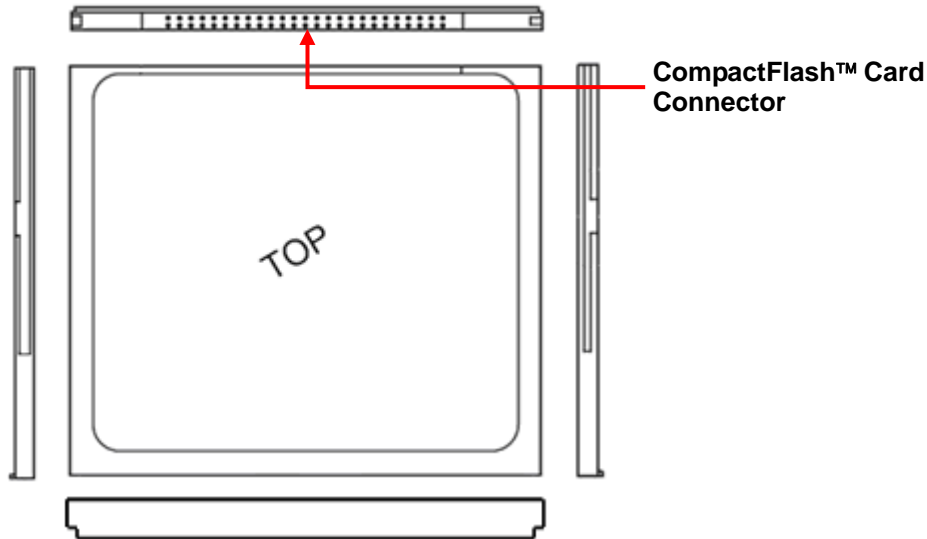
Figure 1: CompactFlash™ Storage Card Overlook Diagram

2.1.2 Dimension

The dimensions of CompactFlash™ Storage Card are illustrated in Figure 2 and described in Table 1.
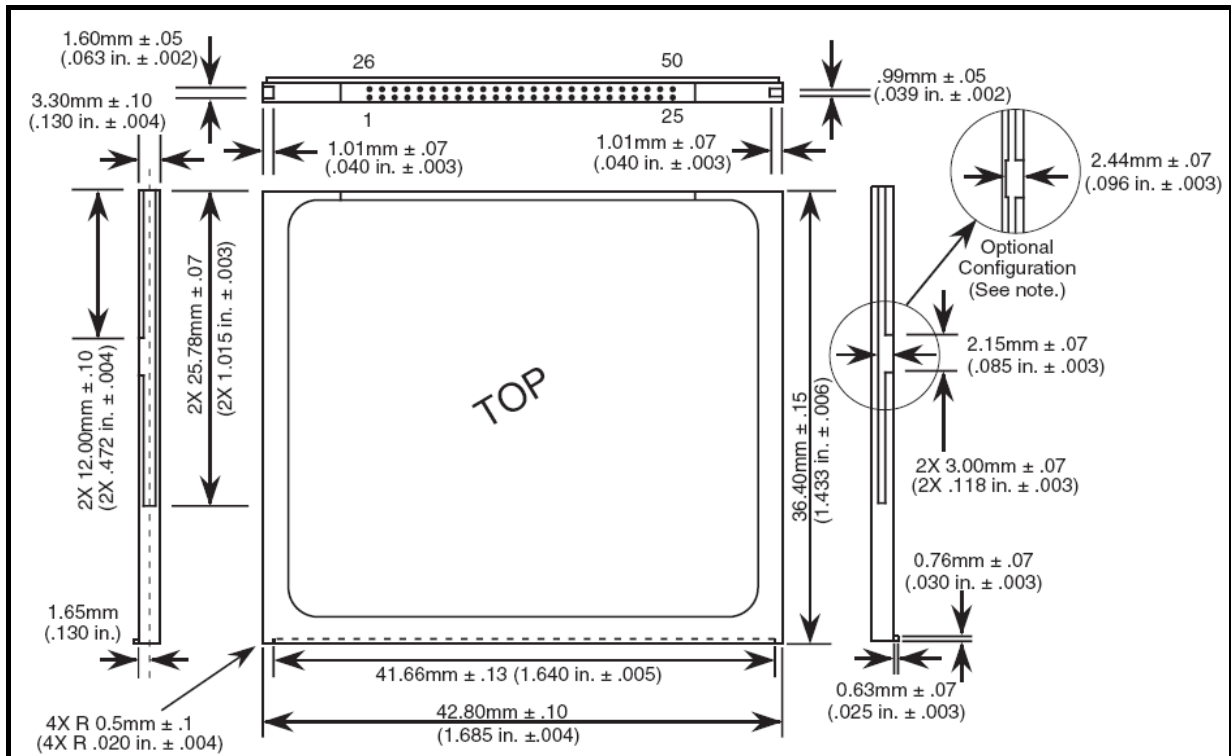
Figure 2: CompactFlash™ Storage Card Dimensions

Notice *The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.*

Table 1: CompactFlash Storage Card Physical Dimension

Length	36.4 ±0.15 mm (1.433 ±0.006in.)
Width	42.8 ±0.10 mm (1.685 ±0.004in.)
Thickness (Including Label Area)	3.3 ±0.10mm (0.13 ±0.004in)

2.1.3 Weight

● Weight: <12g

2.2 Electronic Specifications

2.2.1 Product Definition

The CompacFlash™ Storage Card contains a single chip controller and flash memory module(s) in a matchbook-size package with a 50-pin connector consisting of two rows of 25 female contacts each on 50 mil (1.27mm) centers. The controller interfaces with a host system allowing data to be written to and read from the flash memory modules(s).
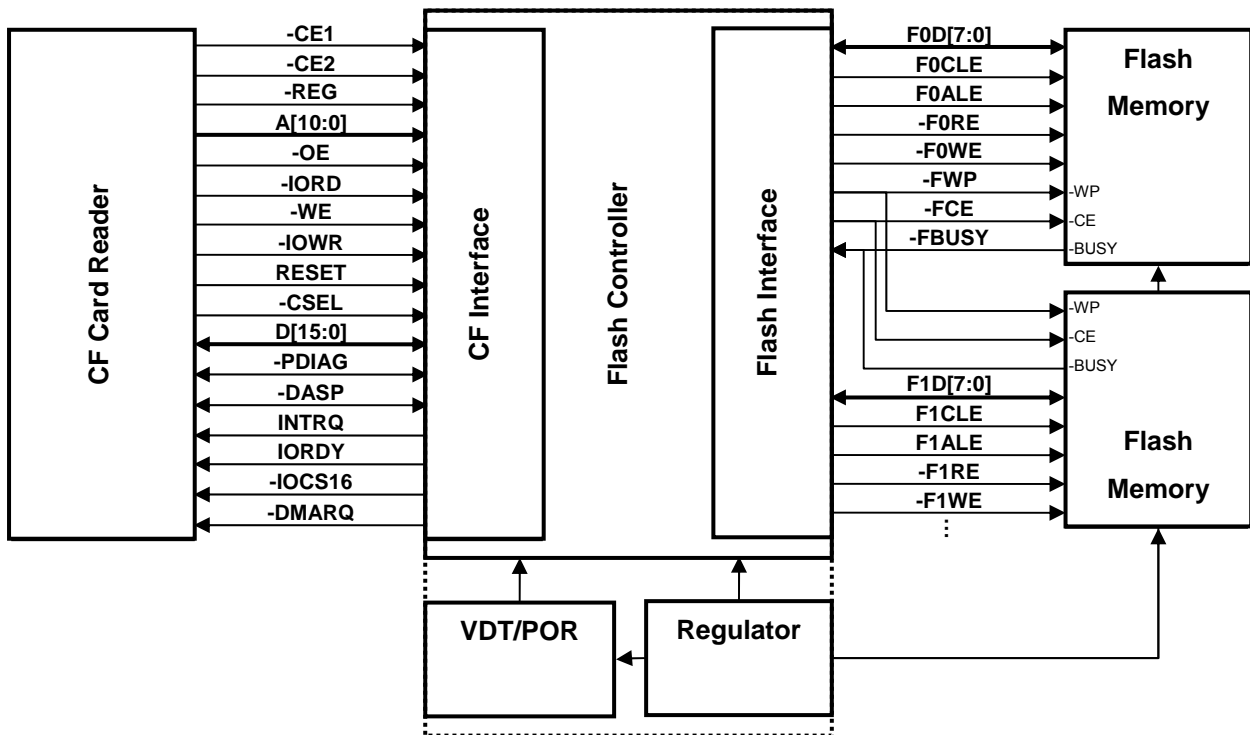
Figure 3: CompactFlash™ Storage Card Block Diagram

2.2.2 Operating Voltage

● Voltage DC +3.3V ± 5% or DC +5.0V ± 10%

2.2.3 Capacity and Block Size information

● Capacity: 128MB ~ 16GB

● Sector Size: 512B

2.2.4 Power Consumption (3.3V/5.0V)

● Current Information (maximum loading)

Test Item	3.3V	5.0V
Write Current	70mA	95mA
Read Current	60mA	85mA
Sleep Current	0.4mA	0.4mA

2.3 Performance Specifications

2.3.1 Modes

4. Memory Card Mode

5. True-IDE Mode (PIO Mode: 6, Multi word DMA Mode: 4, Ultra DMA Mode: 4)

2.3.2 Data Transfer Time

Dual Mode

● Sequential Read: Up to 40 MB/sec

● Sequential Write: Up to 20 MB/sec

Single Mode

● Sequential Read: Up to 20 MB/sec

● Sequential Write: Up to 10 MB/sec

※ *Test Platform:*

MB 1: DFI CF4 / Chipset nForce SLI-DR / CPU: AMD146 2.0GHz DDR400: 256MB

MB 2: GIGA 8I945GME / Chipset: Intel 945+ICH7 /CPU: P4-3.0GHz DDR400: 512MBx2

Testing Software: HD Bench 3.4 / SiSoftware Sandra / Qbench

Testing Operating System: DOS, WinXP, Vista

Notice : *The value is various bases on the testing platform.*

2.3.3 Data Retention

● 10 years without requiring power support

2.3.4 Wear-leveling

● Global Wear-Leveling

2.3.5 Bad Block Management

● The Bad Blocks of Flash Memory will be replaced into new ones by controller.

2.4 Environmental Specification

2.4.1 Temperature

● Operating Temperature: 0ºC to +70ºC, Non Operating Temperature: -40ºC to +85ºC (Industrial type)

● Operating Temperature: -40ºC to +85ºC, Non Operating Temperature: -55ºC to +95ºC (Wide temperature type)

2.4.2 Humidity

● Operating Humidity (30ºC Max. Wet Bulb Temp): 10% to 95%

- Non-Operating Humidity (30ºC Max. Wet Bulb Temp): 10% to 95% (with no condensation relative humidity)

2.4.3 Bare Drop Testing

- Testing Conditions: 75cm height
- Testing Orientation: (Free fell) Front/Rear/Right/Left/Top/Bottom side

2.4.4 Vibration

- Random Vibration (Operation) : Testing Specification

Frequency (Hz)	PSD (G2/Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.01		
100	0.08	6Grms	30min per axis (X・Y・Z)
500	0.08		

- Sine Vibration (Non-Operating): Testing Specification

Frequency (Hz)	PSD (G2/Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.1		
100	0.04	15Grms	30min per axis (X・Y・Z)
500	0.04		
2000	0.004		

- Frequency Range: 3 ~ 2000Hz

2.5 Reliability Specification

2.5.1 ECC (Error Correction Code)

- Built-in Reed Solomon 4symbol/512 bytes

2.5.2 Read and Program/Erase Cycle

- Read: No Limitation
- Program/Erase: 2,000,000 times

2.5.3 MTTF (Mean Time To Failure)

- 2,000,000 hours

2.6 Compliance Specifications

- CE
- FCC

   Notice : *Please contact your closest CSS office for other certificate information*

3. Function

3.1 Pin Signal Assignment

The signals assigned for CF Card applications are described in Figure 4 and Table 2;

Figure 4: CompactFlash Storage Card Signal Connector

Table 2: Compact Flash Storage Card Pin Assignment

Pin NO.	PC Card Memory Mode		PC Card I/O Mode		True IDE Mode	
	Signal name	*I/O*	*Signal name*	*I/O*	*Signal name*	*I/O*
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CS0	I
8	A10	I	A10	I	A10	I
9	-OE	I	-OE	I	-ATA SEL	I
10	A9	I	A9	I	A9	I
11	A8	I	A8	I	A8	I
12	A7	I	A7	I	A7	I
13	VCC	—	VCC	—	VCC	—
14	A6	I	A6	I	A6	I
15	A5	I	A5	I	A5	I
16	A4	I	A4	I	A4	I
17	A3	I	A3	I	A3	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOIS16	O	-IOIS16	O
25	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	-CE2	I	-CE2	I	-CS1	I
33	-VS1	O	-VS1	O	-VS1	O
34	-IORD	I	-IORD	I	-IORD HSTROBE -HDMARDY	I
35	-IOWR	I	-IOWR	I	-IOWR STOP	I
36	-WE	I	-WE	I	-WE	I
37	READY	O	-IREQ	O	INTRQ	O
38	VCC	—	VCC	—	VCC	—
39	-CSEL	I	-CSEL	I	-CSEL	I
40	-VS2	O	-VS2	O	-VS2	O
41	RESET	I	RESET	I	-RESET	I
42	-WAIT	O	-WAIT	O	IORDY -DDMARDY DSTROBE	O
43	-INPACK	O	-INPACK	O	DMARQ	O
44	-REG	I	-REG	I	DMACK	I

Pin NO.	PC Card Memory Mode		PC Card I/O Mode		True IDE Mode	
	Signal name	I/O	Signal name	I/O	Signal name	I/O
45	BVD2	I/O	-SPKR	I/O	-DASP	I/O
46	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	—	GND	—	GND	—

3.2 Card Pin Signal Description

Table 3: CompactFlash Storage Card Pin Signal Description

Signal Name	Dir.	Pin No.	Description
A10 - A0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the-REG signal are used to selectthe following: The I/O port address registers within the CompactFlash Storage Card or CF + Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card , a byte in the card's information structure and its configuration control and status registers.
A10 - A0 (PC Card I/O Mode)			This Signal is the same as the PC Card Memory Mode signal.
A2 - A0 (True IDE Mode)		18,19,20	In True IDE Mode only A [2:0] are used to select the one of eight registers in the Task File. The remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as BVD1 is not supported.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the READY and Write Protect states; while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card / I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1,-CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompcatFlash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket.
-CD1,-CD2 (PC Card Memory Mode)			This signal is the same for all modes.
-CD1,-CD2 (PC Card Memory Mode)			This signal is the same for all modes.

Signal Name	Dir.	Pin No.	Description
-CE1,-CE2 (PC Card I/O Mode) -CE1,-CE2 (PC Card I/O Mode) Card Enable -CS0,-CS1 (True IDE Mode)	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0,-CE1,-CE2 allows 8 bit hosts to access all data on D0 to D7. This Signal is the same as the PC Card Memory Mode signal. In the True IDE Mode -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
-CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode) -CSEL (True IDE Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode) D15 - D00 (PC Card I/O Mode) D15 - D00 (True IDE Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2,23, 22,21	These lines carry the Data, Commands and Status information between the host and the controller.D00 is the LSB of the Even Byte of the Word.D08 is the LSB of the Odd Byte of the Word. This Signal is the same as the PC Card Memory Mode signal. In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode) GND (PC Card I/O Mode) GND (True IDE Mode)	—	1,50	Ground. This signal is the same for all modes. This signal is the same for all modes.

Signal Name	Dir.	Pin No.	Description
-INPCAK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU.
-DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, i.e., the device shall wait until the host asserts –DMACK before negating DMARQ, and reasserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and-CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that dose not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE modes as long as this does not prevent proper operation in any mode.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF +Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode) Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode DMA read is active, this signal has same function as in PC Card I/O Mode.
-HDMARDY (True IDE Mode – In Ultra DMA Protocol DMA Read)			In True IDE Mode when Ultra DMA mode DMA Read is active, This signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer.
HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)			In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.

Signal Name	Dir.	Pin No.	Description
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompcatFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface.
			The clocking shall occur on the negative to positive edge of the signal (Trailing edge)
-IOWR (True IDE Mode – Except Ultra DMA Protocol)			In True IDE Mode, While Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (True IDE Mode – Ultra DMA Protocol Active)			In true IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode. This signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy.
			At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time.
			Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled, Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy sate.
-IREQ (PC Card I/O Mode)			I/O Operation - After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as interrupt Request. This line is strobe low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high interrupt Request to the host.

Signal Name	Dir.	Pin No.	Description
-REG (PC Card Memory Mode) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to Initiate DMA transfers.
			While DMA operations are not active, the card shall ignore the –DMACK signal, including a floating condition.
			If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host.
			A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA Mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
RESET (PC Card Memory Mode)	I	41	The CompactFlash Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception:
			The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card, Under either of these conditions, the card shall emerge from power-up having completed an initial Reset.
			The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode, This input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	—	13,38	+5V +3.3V power.
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode)	O	33,40	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host that the CompactFlash Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is the same for all modes.

Signal Name	Dir.	Pin No.	Description
-WAIT (PC Card Memory Mode)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card Memory Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE mode – Except Ultra DMA mode)			In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
-DDMARDY (True IDE mode – Ultra DMA Write mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer.
-DSTROBE (True IDE mode – Ultra DMA Read mode)			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host, The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured I the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	24	Memory Mode - The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation - When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

3.3 Card Configuration

3.3.1 Attribute Memory Function

Attribute memory is a space where CompactFlash Storage Card. identification and configuration information are stored, and is limited to 8 bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash Storage Cards, the base address of the card configuration registers is 200h.

For the Attribute Memory Read function, signals -REG and -OE shall be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 4: Attribute Memory Function below for signal states and bus validity for the Attribute Memory function.

Table 4: Attribute Memory Function

Function Mode	-REG	-CE2	-CE1	A10	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	X	High Z	High Z
Read Byte Access (8-bit)	L	H	L	L	L or H	L	L	H	High Z	Even Byte
	L	H	L	L	X	H	L	H	High Z	Invalid
Read Word Access (16-bit)	L	L	L	L	L or H	X	L	H	Invalid	Even Byte
Read Odd Byte Access (8-bit)	L	L	H	L	X	X	L	H	Invalid	High Z

Notice: *The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.*

3.3.2 I/O Transfer Function

The I/O transfer to or from the CompactFlash Storage can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Storage. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Storage, the system shall generate a pair of 8 bit references to access the word's even byte and odd byte. The CompactFlash Storage Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Storage responds.

The CompactFlash Storage may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 5: PCMCIA Mode I/O Function

Function Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L	H	L	L	L	H	High Z	Even-Byte
	L	H	L	H	L	H	High Z	Odd-Byte
Byte Output Access (8 bits)	L	H	L	L	H	L	Don't Care	Even-Byte
	L	H	L	H	H	L	Don't Care	Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

3.3.3 Common Memory Transfer Function

The Common Memory transfer to or from the CompactFlash Storage can be either 8 or 16 bits.The CompactFlash Storage Card permit both 8 and 16 bit accesses to all of its Common Memory addresses.

The CompactFlash Storage Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 6: Common Memory Function

Function Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

3.3.4 True IDE Mode I/O Transfer Function

The CompactFlash Storage Card can be configured in a True IDE Mode of operation. The CompactFlash Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. Optionally, CompactFlash Storage Cards may support the following optional detection methods:

1. The card is permitted to monitor the –OE (-ATA SEL) signal at any time(s) and switch to PCMCIA mode upon detecting a high level on the pin.

2. The card is permitted to re-arbitrate the interface mode determination following a transition of the (-) RESET pin.

3. The card is permitted to monitor the –OE (-ATA SEL) signal at any time(s) and switch to True IDE mode upon detection of a continuous low level on pin for an extended period of time.

Host implementers should not rely on any of these optional detection methods in their designs. In the True IDE Mode, the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode, no Memory or Attribute Registers are accessible to the host. CompactFlash Storage Cards permit 8 bit PIO mode data accesses if the user issues a Set Feature Command to put the CompactFlash Storage Card in 8 bit Mode.

Notice: *Removing and reinserting the CompactFlash Storage Card while the host computer's power is on will reconfigure the CompactFlash Storage Card to PC Card ATA mode from the original True IDE Mode. To configure the CompactFlash Storage Card in True IDE Mode, the 50-pin socket is power cycled with the CompactFlash Storage Card inserted and -OE (output enable) asserted.*

Table 7: True IDE mode I/O Function

Function Codes	-CS1	-CS0	A0-A2	-DMACK	-IORD	-IOWR	D15-D8	D7-D0
Invalid Modes	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined in	Undefined in
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined in	Undefined in
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	L	H	High Z	Data Out
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte in	Even-Byte In
DMA Data Register Write	H	H	X	L	H	L	Odd-Byte in	Even-Byte In
Ultra DMA Data Register Write	H	H	X	L	See Note 2		Odd-Byte in	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Ultra DMA Data Register Read	H	H	X	L	See Note 3		Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address[1]	L	H	7h	H	L	H	High Z	Data Out

Notice:

1) Implemented for backward compatibility. Bit D7 of the register shall remain High Z to prevent conflict with any floppy disk controller at the same address. The host software should not rely on the contents of this register.

2) In Ultra DMA Data Register Write mode the signals –IORD, –IOWR and IORDY are redefined and used as follows: –IORD as HSTROBE, –IOWR as STOP and IORDY as –DDMARDY. Data transfers with each edge of HSTROBE. See Section 4.10: True IDE Ultra DMA Mode Read/Write Timing Specification for complete information.

3) In Ultra DMA Data Register Read mode the signals –IORD, –IOWR and IORDY are redefined and used as follows: –IORD as –HDMARDY H, –IOWR as STOP and IORDY as DSTROBE. Data transfers with each edge of DSTROBE. See Section 4.10: True IDE Ultra DMA Mode Read/Write Timing Specification for complete information.

3.4 Card Capacity and Cylinder, Head, Sector

The table 8 show various capacities available for HAK40 series, if your platform does not support auto-detection function or HAK40 series is not identified, we advice can following below Cylinders, Heads, Sectors number to setting your platform.

Table 8: Card Capacity and Cylinder, Head, Sector

Unformatted Disk Capacity	No. of Cylinders	No. of Heads	No. of Sectors	Disk Total Sector
128MB	994	8	32	254,464
256MB	974	16	32	498,688
512MB	1,012	16	63	1,020,096
1GB	1,984	16	63	1,999,872
2GB	3,980	16	63	4,011,840
4GB	7,970	16	63	8,033,760
8GB	15,945	16	63	16,072,560
The following capacity are in LBA mode				
16GB	-16,383	16	63	32,165,280

3.5 Support CFA-ATA Command Set List

CFA-ATA Command Set

- CFA-ATA Command Set summarizes the CFA/ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 9: CFA-ATA Command Set

No	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
2	Erase Sector(s)	C0h	-	Y	Y	Y	Y	Y
3	Execute Drive Diagnostic	90h	-	-	-	-	D	-
4	Flush Cache	E7h	-	-	-	-	D	-
5	Format Track	50h	-	Y	-	Y	Y	Y
6	Identify Device	ECh	-	-	-	-	D	-
7	Identify Device DMA	EEh	-	-	-	-	D	-
8	Idle	E3h or 97h	-	Y	-	-	D	-
9	Idle Immediate	E1h or 95h	-	-	-	-	D	-
10	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
11	Media Lock	DEh	-	-	-	-	D	-
12	Media Unlock	DFh	-	-	-	-	D	-
13	NOP	00h	-	-	-	-	D	-
14	Read Buffer	E4h	-	-	-	-	D	-
15	Read DMA	C8h	-	Y	Y	Y	Y	Y
16	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
17	Read Multiple	C4h	-	Y	Y	Y	Y	Y
18	Read Native Max Address	F8h	-	-	-	-	D	-
19	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
20	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
21	Recalibrate	1Xh	-	-	-	-	D	-
22	Request Sense	03h	-	-	-	-	D	-
23	Seek	7Xh	-	-	Y	Y	Y	Y
24	Set Features	EFh	Y	-	-	-	D	-
25	Set Max Address	F9h	-	Y	Y	Y	Y	Y
26	Set Multiple Mode	C6h	-	Y	-	-	D	-
27	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
28	SMART	B0h	Y	Y	-	Y	Y	-
29	Standby	E2h or 96h	-	-	-	-	D	-
30	Standby Immediate	E0h or 94h	-	-	-	-	D	-
31	Translate Sector	87h	-	Y	Y	Y	Y	Y
32	Wear Level	F5h	-	-	-	-	D	-
33	Write Buffer	E8h	-	-	-	-	D	-
34	Write DMA	CAh	-	Y	Y	Y	Y	Y
35	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
36	Write Multiple	C5h	-	Y	Y	Y	Y	Y
37	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
38	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
39	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
40	Write Verify	3Ch	-	Y	Y	Y	Y	Y

Definitions:

FR = Features Register

SC = Sector Count Register

SN = Sector Number Register

CY = Cylinder Registers

DH = Device/Drive/Head Register

LBA = Logical Block Address Mode Supported (see command descriptions for use).

Y - The register contains a valid parameter for this command. For the Drive/Head Register Y means both the device and head parameters are used.

D - only the device parameter is valid and not the head parameter; C – The register contains command specific data (see command descriptions for use).

(1) Check Power Mode - 98h or E5h

Bit ->	7	6	5	4	3	2	1	0
Command	98h or E5h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Check Power Mode

This command checks the power mode.

If the device is in, going to, or recovering from the sleep mode, the device sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the device is in Idle mode, the device sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

(2) Erase Sector(s) - C0h

Bit ->	7	6	5	4	3	2	1	0
Command	C0h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Erase Sector

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

(3) Execute Drive Diagnostic - 90h

Bit ->	7	6	5	4	3	2	1	0
Command	90h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Execute Drive Diagnostic

This command performs the internal diagnostic tests implemented by the device.

When the diagnostic command is issued, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The Diagnostic codes shown in Table 10: Diagnostic Codes are returned in the Error Register at the end of the command.

Table 10: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

(4) Flush Cache – E7h

Bit ->	7	6	5	4	3	2	1	0
Command	E7h							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Flush Cache

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the Flash memory. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

(5) Format Track - 50h

Bit ->	7	6	5	4	3	2	1	0
Command	50h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Count (LBA mode only)							
Feature (1)	X							

Format Track

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the device expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the device. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

(6) Identify Device – ECh

Bit ->	7	6	5	4	3	2	1	0
Command	ECh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Identify Device

The Identify Device command enables the host to receive parameter information from the device. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 11. All reserved bits or words are zero. Hosts should not depend on obsolete words in Identify Device containing 0. Table 11 specifies each field in the data returned by the Identify Device Command. In Table 11, X indicates a numeric nibble value specific to the device and aaaa indicates an ASCII string specific to the particular drive.

Table 11: Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	0XXX	2	General configuration – Bit Significant with ATA definitions.
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Reserved for vendor
5	0200h	2	Reserved for vendor
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Reserved for assignment by the CFA
9	0000h	2	Reserved
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0002h	2	Reserved for vendor
21	000Xh	2	Reserved for vendor
22	0004h	2	Reserved for vendor
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	800Xh	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0F00h	2	Capabilities: DMA, LBA, IORDY supported
50	0000h	2	Capabilities: Others, Fixed
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	Reserved

Word Address	Default Value	Total Bytes	Data Field Type Information
53	0007h	2	Data Fields 54 to 58, 64 to 70 and 88 are valid
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	010Xh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0X0Xh	2	Multiword DMA transfer.
64	0003h	2	Advanced PIO modes 3 and 4 supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word.
66	0078h	2	Recommended Multiword DMA transfer cycle time.
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80	0020h	2	Major version number, ATA-5 support
81	0000h	2	Minor version number, not reported
82	7409h	2	Features/command sets supported (NOP, SMART,…)
83	5004h	2	Features/command sets supported (Flush Cache, …)
84	4000h	2	Features/command sets supported (extension)
85	740Xh	2	Features/command sets enabled (NOP, SMART,…)
86	X004h	2	Features/command sets enabled (Flush Cache, …)
87	4000h	2	Features/command sets enabled (extension)
88	XXXXh	2	Ultra DMA Mode Supported and Selected
89-92	0000h	8	Reserved
93	XXXXh	2	Hardware Reset result
94-129	0000h	72	Reserved
130-152	XXXXh	8	Reserved for vendor
153-159	0000h	12	Reserved
160	A064h	2	Power requirement description
161-175	XXXXh	2	Reserved for assignment by the CFA
176-254	0000h	180	Reserved
255	XXA5h	2	Integrity Word

Word 0: General Configuration

This field indicates the general characteristics of the device.

Bit 15-12: Configuration Flag: It is fixed as 0 to represent it is an ATA device.

Bits 11-8: Retired. These bits have retired ATA bit definitions. It is recommended that the value of these bits be either the preferred value of 0h or the value of 4h that preserves the corresponding bits to one or zero.

Bit 7: Removable Media Device If Bit 7 is set to 1, the device contains media that can be removed during device operation. If Bit 7 is set to 0, the device contains non-removable media.

Bit 6: Not Removable Controller and/or Device

Alert! *This bit will be considered for obsolescence in a future revision of this standard.*

If Bit 6 is set to 1, the Device is intended to be nonremovable during operation. If Bit 6 is set to 0, the Device is intended to be removable during operation.

Bits 5-0: Retired/Reserved

> `Alert!` *Bit 2 will be considered for definition in a future revision of this standard and shall be 0 at this time.*

Bits 5-1 have retired ATA bit definitions.

Bit 2 shall be 0.

Bit 0 is reserved and shall be 0.

Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

Words 10-19: Serial Number

This field contains the serial number for this device and is right justified and padded with spaces (20h).

Words 20: Buffer type

This field contains the buffer type of the device. It is set by default.

> `Alert!` *This word is considered for obsolescence in a future revision of this standard.*

Words 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

Words 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

Word 47: Read/Write Multiple Sector Count

Bits 15-8 shall be the recommended value of 80h or the permitted value of 00h.   Bits 7-0 of this word define the maximum number of sectors per block that the device supports for Read/Write Multiple commands.

Word 49: Capabilities

Bit 13: Standby Timer

If bit 13 is set to 1 then the Standby timer is supported as defined by the IDLE command

If bit 13 is set to 0 then the Standby timer operation is defined by the vendor.

Bit 11: IORDY Supported

If bit 11 is set to 1 then this device supports IORDY operation.

If bit 11 is set to 0 then this device may support IORDY operation.

Bit 10: IORDY may be disabled

Bit 10 shall be set to 0, indicating that IORDY may not be disabled.

Bit 9: LBA supported

Bit 9 shall be set to 1, indicating that this device supports LBA mode addressing.   Devices shall support LBA addressing.

Bit 8: DMA Supported

If bit 8 is set to 1 then Read DMA and Write DMA commands are supported.

Bit 8 shall be set to 0. Read/Write DMA commands are not currently permitted on CF devices.

Word 51: PIO Data Transfer Cycle Timing Mode

The PIO transfer timing for each device falls into modes that have unique parametric timing specifications. The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2. Values 03h through FFh are reserved.

Word 53: Translation Parameters Valid

Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders heads and sectors. If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid. Any device that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.

Words 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Words 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

Word 59: Multiple Sector Setting

Bits 15-9 are reserved and shall be set to 0.

Bit 8 shall be set to 1 indicating that the Multiple Sector Setting is valid.

Bits 7-0 are the current setting for the number of sectors that shall be transferred per interrupt on Read/Write Multiple commands.

Words 60-61: Total Sectors Addressable in LBA Mode

This field contains the total number of user addressable sectors for the device in LBA mode only.

Word 63: Multiword DMA transfer

Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the device to indicate the multiword DMA mode which is currently selected. Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been

selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected. Selection of Multiword DMA modes 3 and above are specific to device are reported in word 163 as described in Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the Multiword DMA modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the device supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the device supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the device supports Multiword DMA modes 2, 1 and 0.

Support for Multiword DMA modes 3 and above are specific to device are reported in Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

Word 64: Advanced PIO transfer modes supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the advanced PIO modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the device supports PIO mode 3. Bit 1, if set to one, indicates that the device supports PIO mode 4.

Support for PIO modes 5 and above are specific to device are reported in word 163 as described in Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

Word 65: Minimum Multiword DMA transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, and the device guarantees data integrity during the transfer.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all device supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Device shall return a value of zero in this field.

Word 66: Recommended Multiword DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the device will need to negate the DMARQ signal during the transfer of a sector.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all device supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Device shall return a value of zero in this field.

Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any device that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any device that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the device.

If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by device prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.

If bit 1 of word 82 is set to one, the Security Mode feature set is supported.

Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.

Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.

Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.

If bit 5 of word 82 is set to one, write cache is supported.

If bit 6 of word 82 is set to one, look-ahead is supported.

Bit 7 of word 82 shall be set to zero; release interrupt is not supported.

Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.

Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.

Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.

Bit 11 of word 82 is obsolete.

Bit 12 of word 82 shall be set to one; the device supports the Write Buffer command.

Bit 13 of word 82 shall be set to one; the device supports the Read Buffer command.

Bit 14 of word 82 shall be set to one; the device supports the NOP command.

Bit 15 of word 82 is obsolete.

Bit 0 of word 83 shall be set to zero; the device does not support the Download Microcode command.

Bit 1 of word 83 shall be set to zero; the device does not support the Read DMA Queued and Write DMA Queued commands.

Bit 2 of word 83 shall be set to one; the device supports the CFA feature set.

If bit 3 of word 83 is set to one, the device supports the Advanced Power Management feature set.

Bit 4 of word 83 shall be set to zero; the device does not support the Removable Media Status feature set.

Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by device prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.

If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security Set Password command.

Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.

Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.

Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.

If bit 5 of word 85 is set to one, write cache is enabled.

If bit 6 of word 85 is set to one, look-ahead is enabled.

Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.

Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.

Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.

Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.

Bit 11 of word 85 is obsolete.

Bit 12 of word 85 shall be set to one; the device supports the Write Buffer command.

Bit 13 of word 85 shall be set to one; the device supports the Read Buffer command.

Bit 14 of word 85 shall be set to one; the device supports the NOP command.

Bit 15 of word 85 is obsolete.

Bit 0 of word 86 shall be set to zero; the device does not support the Download Microcode command.

Bit 1 of word 86 shall be set to zero; the device does not support the Read DMA Queued and Write DMA

Queued commands.

If bit 2 of word 86 shall be set to one, the device supports the CFA feature set.

If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.

Bit 4 of word 86 shall be set to zero; the device does not support the Removable Media Status feature set.

Word 88: Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported.

Bits 15-13: Reserved

Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected

Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected

Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected

Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected

Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected

Bits 7-5: Reserved

Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 shall be set to 1.

Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 shall be set to 1.

Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 shall be set to 1.

Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 shall be set to 1.

Bit 0: 1 = Ultra DMA mode 0 is supported

Word 93: Hardware Configuration test results

During hardware reset execution, Device 0 shall clear bits 13-8 of this word to zero and shall set bits 7-0 of the word as indicated to show the result of the hardware reset execution. During hardware reset execution, Device 1 shall clear bits 7-0 of this word to zero and shall set bits 13-8 as indicated to show the result of the hardware reset execution.

Bit 13 shall be set or cleared by the selected device to indicate whether the device detected CBLID- above VIH or below VIL at any time during execution of each IDENTIFY DEVICE routine after receiving the command from the host but before returning data to the host. This test may be repeated as desired by the device during command execution (see Annex B).Word 89 specifies the time required for the Security Erase Unit command to complete. This command shall be supported on devices that support security.

Notice: *CBLID- is grounded in the 80-conductor cable assembly host connector for the purpose of indicating to the host that the cable assembly being used is an 80-conductor assembly not a 40-conductor assembly.*

The contents of bits 12-0 of this word shall change only during the execution of a hardware reset.

Bit 15: Shall be cleared to zero.

Bit 14: Shall be set to one.

Bit 13: 1 = dvice detected CBLID- above ViH

0 = device detected CBLID- below ViL

Bit 12-8: Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:

Bit 12: Reserved.

Bit 11:   0 = Device 1 did not assert PDIAG-.

1 = Device 1 asserted PDIAG-.

Bit 10-9: These bits indicate how Device 1 determined the device number:

00 = Reserved.

01 = a jumper was used.

10 = the CSEL signal was used.

11 = some other method was used or the method is unknown.

Bit 8: Shall be set to one.

Bit 7-0: Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:

Bit 7: Reserved.

Bit 6: 0 = Device 0 does not respond when Device 1 is selected.

1 = Device 0 responds when Device 1 is selected.

Bit 5: 0 = Device 0 did not detect the assertion of DASP-.

1 = Device 0 detected the assertion of DASP-.

Bit 4: 0 = Device 0 did not detect the assertion of PDIAG-.

1 = Device 0 detected the assertion of PDIAG-.

Bit 3: 0 = Device 0 failed diagnostics.

1 = Device 0 passed diagnostics.

Bit 2-1: These bits indicate how Device 0 determined the device number:

00 = Reserved.

01 = a jumper was used.

10 = the CSEL signal was used.

11 = some other method was used or the method is unknown.

Bit 0: Shall be set to one.

Word 160: Power Requirement Description

This word is required for devices that support power mode 1.

Bit 15: VLD

If set to 1, indicates that this word contains a valid power requirement description.

If set to 0, indicates that this word does not contain a power requirement description.

Bit 14: RSV

This bit is reserved and shall be 0.

Bit 13: -XP

If set to 1, indicates that the device does not have Power Level 1 commands.

If set to 0, indicates that the device has Power Level 1 commands

Bit 12: -XE

If set to 1, indicates that Power Level 1 commands are disabled.

If set to 0, indicates that Power Level 1 commands are enabled.

Bit 0-11: Maximum current

This field contains the device's maximum current in mA.

(7) Identify Device DMA – EEh

Bit ->	7	6	5	4	3	2	1	0
Command	EEh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Identify Device DMA

This command enables the host to receive parameter information from the device in DMA mode. The command transfers the same 256 words of device identification data as transferred by the IDENTIFY DEVICE command. It is an obsolete command after ATA-4.

(8) Idle - 97h or E3h

Bit ->	7	6	5	4	3	2	1	0
Command	97h or E3h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

Idle

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

(9) Idle Immediate - 95h or E1h

Bit ->	7	6	5	4	3	2	1	0
Command	95h or E1h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Idle Immediate

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

(10) Initialize Drive Parameters - 91h

Bit ->	7	6	5	4	3	2	1	0
Command	91h							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

Initialize Drive Parameters

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Device/Drive/Head registers are used by this command.

(11) Media Lock – DEh

Bit ->	7	6	5	4	3	2	1	0
Command	DEh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Media Lock

It is implemented for compatibility and is no function in this device.

(12) Media Unlock – DFh

Bit ->	7	6	5	4	3	2	1	0
Command	DFh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Media Unlock

It is implemented for compatibility and is no function in this device.

(13) NOP – 00h

Bit ->	7	6	5	4	3	2	1	0
Command	00h							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

NOP

This command always fails with an aborted command error.

(14Read Buffer - E4h

Bit ->	7	6	5	4	3	2	1	0
Command	E4h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Read Buffer

The Read Buffer command enables the host to read the current contents of the device's sector buffer. This command has the same protocol as the Read Sector(s) command.

(15 Read DMA – C8h

Bit ->	7	6	5	4	3	2	1	0
Command	C8h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Read DMA

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the device sets BSY, puts all or part of the sector of data in the buffer. The Device is then permitted, although not required, to set DRQ, clear BSY. The Device asserts DMAREQ while data is available to be transferred. The Device asserts DMAREQ while data is available to be transferred. The host then reads the (512 * sector-count) bytes of data from the Device using DMA. While DMAREQ is asserted by the Device, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last

sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Read DMA command is received by the Device and 8 bit transfer mode has been enabled by the Set Features command, the Device shall return the Aborted error.

(16) Read Long Sector - 22h or 23h

Bit ->	7	6	5	4	3	2	1	0
Command	22h or 23h							
C/D/H (6)	1	LBA	1	Drive		Head (LBA 27-24)		
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Read Long Sector

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the device does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

(17) Read Multiple - C4h

Bit ->	7	6	5	4	3	2	1	0
Command	C4h							
C/D/H (6)	1	LBA	1	Drive		Head (LBA 27-24)		
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Read Multiple

Notice: *This specification requires that devices support a multiple block count of 1 and permits larger values to be supported.*

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command. Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = (sector count) modulo (block count).

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

(18) Read Native Max Address – F8h

Bit ->	7	6	5	4	3	2	1	0
Command	F8h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Read Native Max Address

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition. The native maximum address is the maximum address that is valid when using the SET MAX ADDRESS command.

(19) Read Sector(s) - 20h or 21h

Bit ->	7	6	5	4	3	2	1	0
Command	20h or 21h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Read Sector(s)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued

and after each sector of data (except the last one) has been read by the host, the device sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

(20) Read Verify Sector(s) - 40h or 41h

Bit ->	7	6	5	4	3	2	1	0
Command	40h or 41h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Read Verify Sector(s)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the device sets BSY.

When the requested sectors have been verified, the device clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

(21) Recalibrate - 1Xh

Bit ->	7	6	5	4	3	2	1	0
Command	1Xh							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Recalibrate

This command is effectively a NOP command to the device and is provided for compatibility purposes.

(22) Request Sense - 03h

Bit ->	7	6	5	4	3	2	1	0
Command	03h							
C/D/H (6)			X	Drive	x			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Request Sense

This command requests extended error information for the previous command. Table 12 defines the valid extended error codes for the device Series product. The extended error code is returned to the host in the Error Register.

Table 12: Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed
22h	Power Level 1 Disabled

(23) Seek - 7Xh

Bit ->	7	6	5	4	3	2	1	0
Command	7Xh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Seek

This command is effectively a NOP command to the device although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

(24) Set Features – EFh

Bit ->	7	6	5	4	3	2	1	0
Command	EFh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

Set Features

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the Compact Flash Storage Device shall return command aborted. Table 13: Feature Supported defines all features that are supported.

Table 13: Feature Supported

Feature	Operation
01h	Enable 8 bit data transfers.
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Count register.
05h	Enable Advanced Power Management.
09h	Enable Extended Power operations. *(Alert! It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.)*
0Ah	Enable Power Level 1 commands.
44h	Product specific ECC bytes apply on Read/Write Long commands.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	NOP - Accepted for backward compatibility.
81h	Disable 8 bit data transfer.
82h	Disable Write Cache.
85h	Disable Advanced Power Management.
89h	Disable Extended Power operations. *(Alert! It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.)*
8Ah	Disable Power Level 1 commands.
96h	NOP - Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
AAh	Enable Read Look Ahead.
BBh	4 bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers shall occur on the low order D[7:0] data bus and the -IOIS16 signal shall not be asserted for data register accesses.   The host shall not enable this feature for DMA transfers.

Features 02h and 82h allow the host to enable or disable write cache in devices that implement write cache. When the subcommand disable write cache is issued, the device shall initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For Devices which support DMA, one Multiword DMA mode shall be selected at all

times. The host may change the selected modes by the Set Features command.

Table 14: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

If a device supports PIO modes greater than 0 and receives a Set Features command with a Set Transfer Mode parameter and a Sector Count register value of "00000000b", it shall set its default PIO mode. If the value is "00000001b" and the device supports disabling of IORDY, then the device shall set its default PIO mode and disable IORDY. A device shall support all PIO modes below the highest mode supported, e.g., if PIO mode 1 is supported PIO mode 0 shall be supported.

Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.

A device reporting support for Multiword DMA modes shall support all Multiword DMA modes below the highest mode supported. For example, if Multiword DMA mode 2 support is reported, then modes 1 and 0 shall also be supported.

A device reporting support for Ultra DMA modes shall support all Ultra DMA modes below the highest mode supported. For example, if Ultra DMA mode 2 support is reported then modes 1 and 0 shall also be supported.

If an Ultra DMA mode is enabled any previously enabled Multiword DMA mode shall be disabled by the device. If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device. Feature 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a Set Features command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Table15: Advanced power management levels show these values.

Table 15: Advanced power management levels

Level	Sector Count Value
Maximum performance	FEh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	FFh
Reserved	00h

Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h and a higher performance, higher

power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.

Feature 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement Set Features subcommand 05h.

Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the device with extended power.

Features 55h and BBh are the default features for the device; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Feature code 9Ah enables the host to configure the device to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the device should consume. For example, if the Sector Count register were set to 6, the device would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the device responds to the host with the range of values supported by the device. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The device shall accept values outside this programmable range, but shall operate at either the lowest power or highest performance as appropriate.

Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults shall be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

(25) Set Max Address – F9h

Bit ->	7	6	5	4	3	2	1	0
Command	F9h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							Volatile
Feature (1)	X							

Set Max Address

This command is used to set a temporary or permanent maximum address. After successful command completion, all read and write access attempts to addresses greater than the specified maximum address shall be rejected with an IDNF error. IDENTIFY DEVICE response words (61:60) shall reflect the maximum address set with this command.

After a successful SET MAX ADDRESS command using a new maximum LBA the content of all IDENTIFY DEVICE words (61:60) shall be equal to the new Maximum LBA + 1.

The LBA address in the command registers is the maximum address for the setting. Bit 0 in the Sector Count represents Value volatile.

If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset.

If bit 0 is cleared to zero, the device shall revert to the most recent non-volatile maximum address value setting over power-up or hardware reset.

(26) Set Multiple Mode - C6h

Bit ->	7	6	5	4	3	2	1	0
Command	C6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Set Multiple Mode

This command enables the device to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the device sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands.

If the block count is not supported, an Aborted Command error is posted and the Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

(27) Set Sleep Mode- 99h or E6h

Bit ->	7	6	5	4	3	2	1	0
Command	99h or E6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Set Sleep Mode

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds. Note that this time base (5 msec) is different from the ATA Specification.

(28) SMART- B0h

Individual SMART commands are identified by the value placed in the Feature register. The following table shows these Feature register values for this device.

Table 16: SMART Feature register values

Value	Command
D0h	SMART Read Data
D2h	SMART Enable/Disable Attribute Autosave
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status
E0h	(Vendor Specific SMART function): SMART Read Remap Data
E1h	(Vendor Specific SMART function): SMART Read Wear Level Data
Others	Reserved

Notice: *If reserved size below the Threshold, the status can be read from Cylinder register by SMART Return Status command (DAh).*

● **Feature D9h: SMART Disable Operations**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)		X		Drive		X		
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D9h							

SMART Disable Operations

This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature. After command acceptance the device shall disable all SMART operations. SMART data shall no longer be monitored or saved by the device. The state of SMART, either enabled or disabled, shall be preserved by the device across power cycles.

After receipt of this command by the device, all other SMART commands including SMART DISABLE OPERATIONS commands, with the exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be command aborted by the device.

● **Feature D2h: SMART Enable/Disable Attribute Autosave**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)		X		Drive		X		
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	00h or F1h							
Feature (1)	D2h							

SMART Enable/Disable Attribute Autosave

This command enables and disables the optional attribute autosave feature of the device. This command may either allow the device, after some vendor specified event, to save the device updated attribute values to nonvolatile memory; or this command may cause the autosave feature to be disabled. The state of the attribute autosave feature (either enabled or disabled) shall be preserved by the device across power cycles.

A value of zero written by the host into the device's Sector Count register before issuing this command shall cause this feature to be disabled. Disabling this feature does not preclude the device from saving SMART data to non-volatile

memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F1h written by the host into the device's Sector Count register before issuing this command shall cause this feature to be enabled. Any other meaning of this value or any other non-zero value written by the host into this register before issuing this command may differ from device to device. The meaning of any nonzero value written to this register at this time shall be preserved by the device across power cycles.

If this command is not supported by the device, the device shall return command aborted upon receipt from the host.

During execution of the autosave routine the device shall not set BSY to one nor clear DRDY to zero. If the device receives a command from the host while executing the autosave routine the device shall begin processing the command within two seconds.

● **Feature D8h: SMART Enable Operations**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)		X		Drive		X		
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D8h							

SMART Enable Operations

This command enables access to all SMART capabilities within the device. Prior to receipt of this command SMART data are neither monitored nor saved by the device. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any SMART data or functions.

● **Feature D0h: SMART Read Data**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)		X		Drive		X		
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D0h							

SMART Read Data

This command returns the Device SMART data structure to the host. Table showed below defines the 512 bytes that make up the Device SMART data structure.

Table 17: Device SMART Data Structure

Offset	Value	Description
0-1	0004h	SMAT Structure Revision code
2-361	V	Attribute entries 1 to 30 (12 bytes each)
362	00h	Off-line data collection status (No off-line data collection) (Fixed)
363	00h	Self-test execution status byte (Self-test completed) (Fixed)
364-365	0000h	Total time in seconds to complete off-line data collection activity (Fixed)
366	00h	Reserved
367	00h	Off-line data collection capability (No Off-line data collection) (Fixed)
368-369	0003h	SMART capability
370	00h	Error logging capability (No error logging) (Fixed)
371	00h	Reserved
372	00h	Short self-test routine recommended polling time (in minutes) (Fixed)
373	00h	Extended self-test routine recommended polling time (in minutes) (Fixed)
374-385	00h	Reserved
386-387	00h	Reserved
388-395	V	Reserved, vendor specification area
396-510	00h	Reserved
511	V	Data structure checksum

V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.
* 4 Byte value : [MSB] [2] [1] [LSB]

- (0-1) Revision code

   This revision code area defines the firmware revision for the device.

- (2-361) Attribute entries 1 to 30 (12 bytes each)

   There are five attributes that are defined for this device. These return their data in the attribute section of the

   SMART data, using a 12 byte data field. Rest of the area is reserved.

- **Spare Block Count Attribute:** This attribute gives information about the amount of available spare blocks.

Offset	Value	Description
0	196	Attribute ID – Reallocation Count
1-2	0003h	Flags – Pre-fail type, value is updated during normal operation
3	V	Attribute value. The value returned here is the minimum percentage of remaining spare blocks over all flash chips, i.e. min over all chips: (100 × current spare blocks / initial spare blocks)
4-5	V	Initial number of spare blocks of the flash chip that has been used for the attribute value calculation.
6-7	V	Current number of spare blocks of the flash chip that has been used for the attribute value calculation.
8-9	V	Sum of the initial number of spare blocks for all flash chips.
10-11	V	Sum of the current number of spare blocks for all flash chips.

This attribute is used for the SMART Return Status command. If the attribute value field is less than the spare

block threshold, the SMART Return Status command will indicate a threshold exceeded condition.

- **Erase Count Attribute**: This attribute gives information about the amount of flash block erases that have been performed.

Offset	Value	Description
0	229	Attribute ID – Erase Count Usage (vendor specific)
1-2	0003h	Flags – Pre-fail type, value is updated during normal operation
3	V	Attribute value. The value returned here is an estimation of the remaining device life, in percent, based on the number of block erases compared to the target number of erase cycles per flash block.
4-11	V	Estimated total number of block erases

This attribute is used for the SMART Return Status command. If the attribute value field is less than the erase count threshold, the SMART Return Status command will indicate a threshold exceeded condition.

- **Total ECC Errors Attribute:** This attribute gives information about the total number of ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	203	Attribute ID – Number of ECC errors
1-2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4-7	V	Total number of ECC errors (correctable and uncorrectable)
8-11	-	Reserved

- **Correctable ECC Errors Attribute:** This attribute gives information about the total number of correctable ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	204	Attribute ID – Number of corrected ECC errors
1-2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4-7	V	Total number of correctable ECC errors.
8-11	-	Reserved

- Total Number of Reads Attribute: This attribute gives information about the total number of flash read commands. This can be useful for the interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	232	Attribute ID – Number of Reads (vendor specific)
1-2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4-11	V	Total number of flash read commands.

- **UDMA CRC Errors Attribute:** This attribute gives information about the total number of UDMA CRC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	199	Attribute ID – UDMA CRC error rate
1-2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4-7	V	Total number of UDMA CRC errors
8-11	-	Reserved

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- (368-369) SMART capabilities

The following describes the definition for the SMART capabilities bits.

- Bit 0 - If this bit is set to one, the device saves SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode. If this bit is cleared to zero, the device does not save SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode.

- Bit 1 - This bit shall be set to one to indicate that the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

- Bits (15:2) (Reserved).

- (372) Self-test routine recommended polling time

The self-test routine recommended polling time shall be equal to the number of minutes that is the minimum recommended time before which the host should first poll for test completion status. Actual test time could be several times this value. Polling before this time could extend the self-test execution time or abort the test depending on the state of bit 2 of the off-line data capability bits.

- (511) Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

● **Feature DAh: SMART Return Status**

Bit ->	7	6	5	4	3	2	1	0
Command				B0h				
C/D/H (6)		X		Drive		X		
Cyl High (5)				C2h				
Cyl Low (4)				4Fh				
Sec Num (3)				X				
Sec Cnt (2)				X				
Feature (1)				DAh				

SMART Return Status

This command causes the device to communicate the reliability status of the device to the host. If a threshold exceeded condition is not detected by the device, the device shall set the LBA Mid register to 4Fh and the LBA High register to C2h. If a threshold exceeded condition is detected by the device, the device shall set the LBA Mid register to F4h and the LBA High register to 2Ch.

● **Feature E0h: SMART Read Remap Data (Vendor specific)**

Bit ->	7	6	5	4	3	2	1	0
Command				B0h				
C/D/H (6)		X		Drive		X		
Cyl High (5)				C2h				
Cyl Low (4)				4Fh				
Sec Num (3)				X				
Sec Cnt (2)				01h				
Feature (1)				E0h				

SMART Read Remap Data (Vendor specific)

This command returns one sector of spare block information. The information is the initial number of blocks (directly after the pre-format) per flash chip available for bad block remap, and the current number of blocks per flash chip available for bad block remap. The layout of the returned sector is:

Offset	Description
0-31	Initial number of replacement blocks for chips 0..15, 2 bytes per entry
32-63	Current number of replacement blocks for chips 0..15, 2 bytes per entry
64-511	Reserved

● **Feature E1h: SMART Read Wear Level Data (Vendor specific)**

Bit ->	7	6	5	4	3	2	1	0
Command				B0h				
C/D/H (6)		X		Drive		X		
Cyl High (5)				C2h				
Cyl Low (4)				4Fh				
Sec Num (3)				X				
Sec Cnt (2)				04h				
Feature (1)				E1h				

SMART Read Wear Level Data (Vendor specific)

This command will return four sectors of information regarding the status of the wear leveling. The information returned is the distribution of the blocks into the 1024 possible wear level classes. For each of the wear level classes, the number of blocks that have this class is returned in the data sectors.

The layout of the returned sectors is, with n the sector number from 0 to 3:

Offset	Description
0-1	Number of flash blocks that have wear level class 256*n+0
2-3	Number of flash blocks that have wear level class 256*n+1
……	......
508-509	Number of flash blocks that have wear level class 256*n+254
510-511	Number of flash blocks that have wear level class 256*n+255

i.e. the first sector returns the information for wear level classes 0 to 255, the second sector returns the information for wear level classes 256 to 511, and so on.

A block moves from one wear level class into the next when it reaches the number of erases that is specified as the "Wear Level Threshold" in the preformat. A common threshold number is 4095, this means that blocks in wear level class 0 have seen 0 to 4095 erases, blocks in wear level class 1 have seen 4096 to 8191 erases, and so on. Using this information, statements about the wear of the device, and of the estimated remaining life can be made. The useful range of wear level classes is 0 to 1022, class 1023 has blocks that are not subject to wear leveling, like the Anchor block.

(29) Standby - 96h or E2h

Bit ->	7	6	5	4	3	2	1	0
Command	96h or E2h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Standby

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

(30) Standby Immediate - 94h or E0h

Bit ->	7	6	5	4	3	2	1	0
Command	94h or E0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Standby Immediate

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

(31) Translate Sector - 87h

Bit ->	7	6	5	4	3	2	1	0
Command	87h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Translate Sector

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that sector. Table 18 represents the information in the buffer. Please note that this command is unique to the device.

Table 18: Translate Sector Information

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04) - LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h – 17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A) 1
1Bh-1FFh	Reserved

Notice: **1) A value of 0 indicates Hot Count is not supported.**

(32) Wear Level – F5h

Bit ->	7	6	5	4	3	2	1	0
Command	F5h							
C/D/H (6)	X			Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Completion Status							
Feature (1)	X							

Wear Level

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register shall always be returned with a 00h indicating Wear Level is not needed.

(33) Write Buffer - E8h

Bit ->	7	6	5	4	3	2	1	0
Command	E8h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Write Buffer

The Write Buffer command enables the host to overwrite contents of the device's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

(34) Write DMA – CAh

Bit ->	7	6	5	4	3	2	1	0
Command	CAh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write DMA

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the device sets BSY, puts all or part of the sector of data in the buffer. The Device is then permitted, although not required, to set DRQ, clear BSY. The Device asserts DMAREQ while data is available to be transferred. The host then writes the (512 * sector-count) bytes of data to the Device using DMA. While DMAREQ is asserted by the Device, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Write DMA command is received by the Device and 8 bit transfer mode has been enabled by the Set Features command, the Device shall return the Aborted error.

(35) Write Long Sector - 32h or 33h

Bit ->	7	6	5	4	3	2	1	0
Command	32h or 33h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Write Long Sector

This command is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state device, the four bytes of ECC transferred by the host may be used by the device. The device may discard these four bytes and write the sector with valid ECC data. This comm device and has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

(36) Write Multiple Command - C5h

Bit ->	7	6	5	4	3	2	1	0
Command				C5h				
C/D/H (6)	1	LBA	1	Drive		Head		
Cyl High (5)				Cylinder High				
Cyl Low (4)				Cylinder Low				
Sec Num (3)				Sector Number				
Sec Cnt (2)				Sector Count				
Feature (1)				X				

Write Multiple Command

Notice: *This specification requires that devices support a multiple block count of 1 and permits larger values to be supported*.

This command is similar to the Write Sectors command. The device sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block that contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = (sector count) modulo (block count).

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation shall be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector numbers of the sector where the error occurred. The Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command, e.g., each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

(37) Write Multiple without Erase – CDh

Bit ->	7	6	5	4	3	2	1	0
Command				CDh				
C/D/H (6)	X1	LBA	1	Drive		Head		
Cyl High (5)				Cylinder High				
Cyl Low (4)				Cylinder Low				
Sec Num (3)				Sector Number				
Sec Cnt (2)				Sector Count				
Feature (1)				X				

Write Multiple without Erase

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued.

(38) Write Sector(s) - 30h or 31h

Bit ->	7	6	5	4	3	2	1	0
Command	30h or 31h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Sector(s)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the device sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

(39) Write Sector(s) without Erase - 38h

Bit ->	7	6	5	4	3	2	1	0
Command	38h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Sector(s) without Erase

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased with the Erase Sector(s) command, a normal write sector operation will occur.

(40) Write Verify - 3Ch

Bit ->	7	6	5	4	3	2	1	0
Command	3Ch							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Verify

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command.

4. Operation Specification

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	VCC	-0.3 ~ +5.6	V
Input voltage	Vin	-0.3 ~ +5.6	V

Notice: *(Referenced to GND)*

Electric characteristics, Vcc=3.3V±10%, or Vcc=5.0V±10%

Item	Symbol	Min. Value		Max. Value		Unit	Remark
		3.3V.	5V	3.3V	5V		
Input voltage (TTL level)	V_{IH}	2.4 2.1	4.0 2.92		-	V	Non-Schmitt trigger Schmitt trigger
	V_{IL}	- -	- -	0.6 1.25	0.8 1.70	V	Non-Schmitt trigger Schmitt trigger
Output voltage	V_{OH}	2.4	2.4	-	-	V	I_{OH}=-1mA
	V_{OL}	-	-	0.45	0.45	V	I_{OL}=4mA

4.2 Attribute Memory Read Timing

Attribute Memory access time is define as 300 ns. Detailed timing specs are shown in Table 19.

Table 19: Attribute Memory Read Timing

Speed Version			300 ns	
Item (unit: ns)	Symbol	IEEE Symbol	Min	Max
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data valid from Address Change	tv(A)	tAXQX	0	

Notice: *All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card to the system. The –CE signal or both the –OE signal and the –WE signal shall be de-asserted between consecutive cycle operations.*
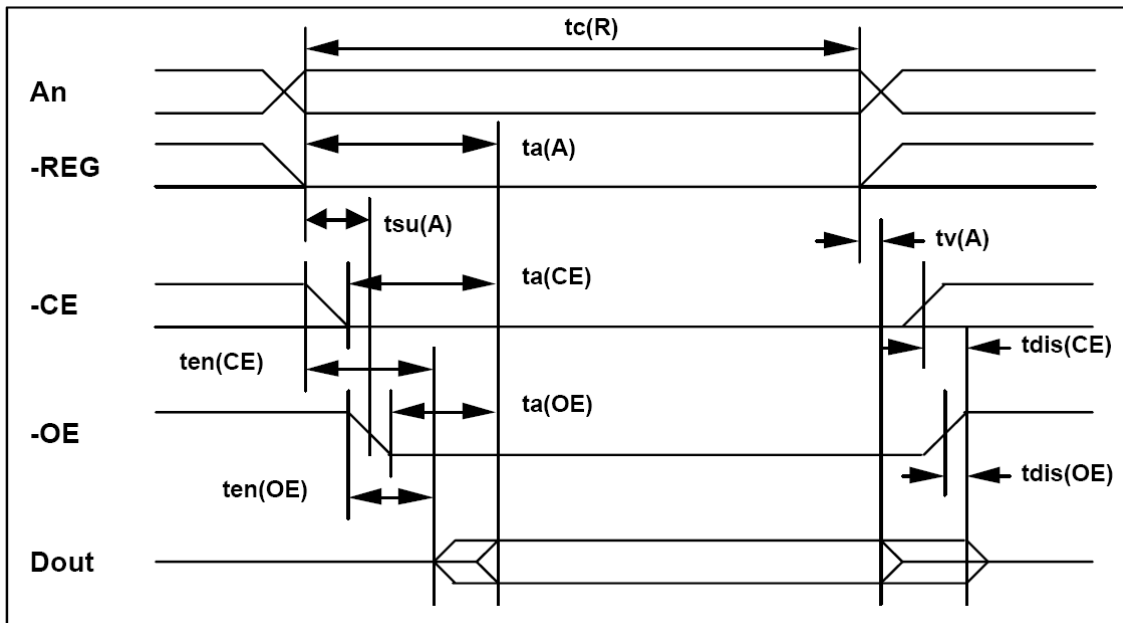
Figure 5: Attribute Memory Read Timing Diagram

4.3 Configuration Register (Attribute Memory) Write Timing

The Card Configuration write access time is defined as 250ns. Detailed timing specifications are shown in Table 20.

Table 20: Configuration Register (Attribute Memory) Write Timing

Speed Version			250 ns	
Item (unit: ns)	Symbol	IEEE Symbol	Min	Max
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	Tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

Notice: *All times are in nanoseconds. Din signifies data provide by the system to the CompactFlash Storage Card.*
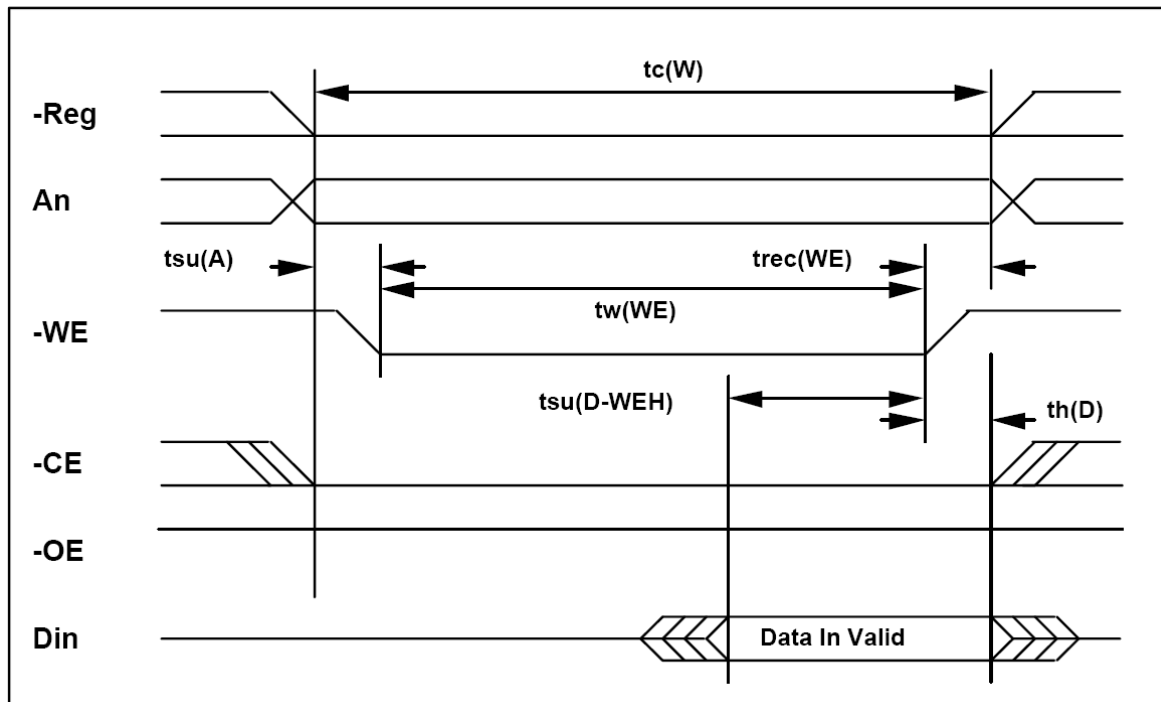
Figure 6: Configuration Register (Attribute Memory) Write Timing Diagram

4.4 Common Memory Read Timing

Table 21: Common Memory Read Timing

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item (unit: ns)	Symbol	IEEE Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE setup Before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35		35		na[1]
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0		0		na[1]
Wait Width Time[2]	tw(WT)	tWTLWTH		350		350		350		na[1]

Notice:

1) –WAIT is not supported in ths mode.

2) The maximum load on –WAIT is 1 LSTTL with 50pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card to the system. The –WAIT signal may be ignored if the –OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card information Structure. The Wait Width time meets the PCMCIA specification of 12us but is intentionally less in this specification.
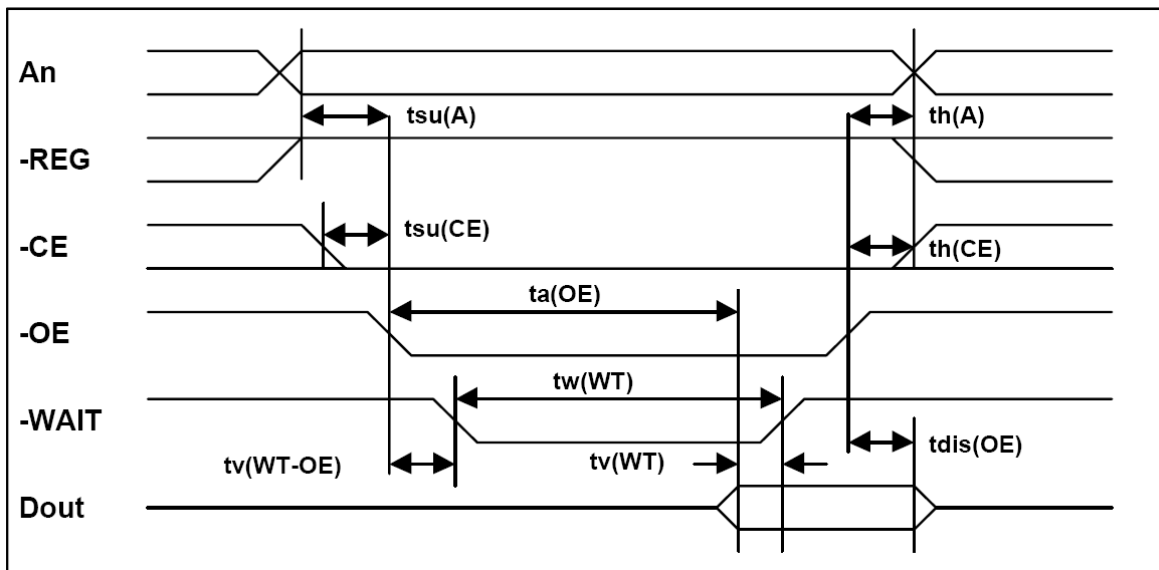
Figure 7: Common Memory Read Timing Diagram

4.5 Common Memory Write Timing

Table 22: Common Memory Write Timing

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item (unit: ns)	Symbol	IEEE Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Setup before WE	tsu(D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35		35		30		na[1]
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		na[1]	
Wait Width Time[2]	tw(WT)	tWTLWTH		350		350		350		na[1]

Notice:

1) –WAIT is not supported in ths mode.

2) The maximum load on –WAIT is 1 LSTTL with 50pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The –WAIT signal may be ignored if the –WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card information Structure. The Wait Width time meets the PCMCIA specification of 12us but is intentionally in this specification.
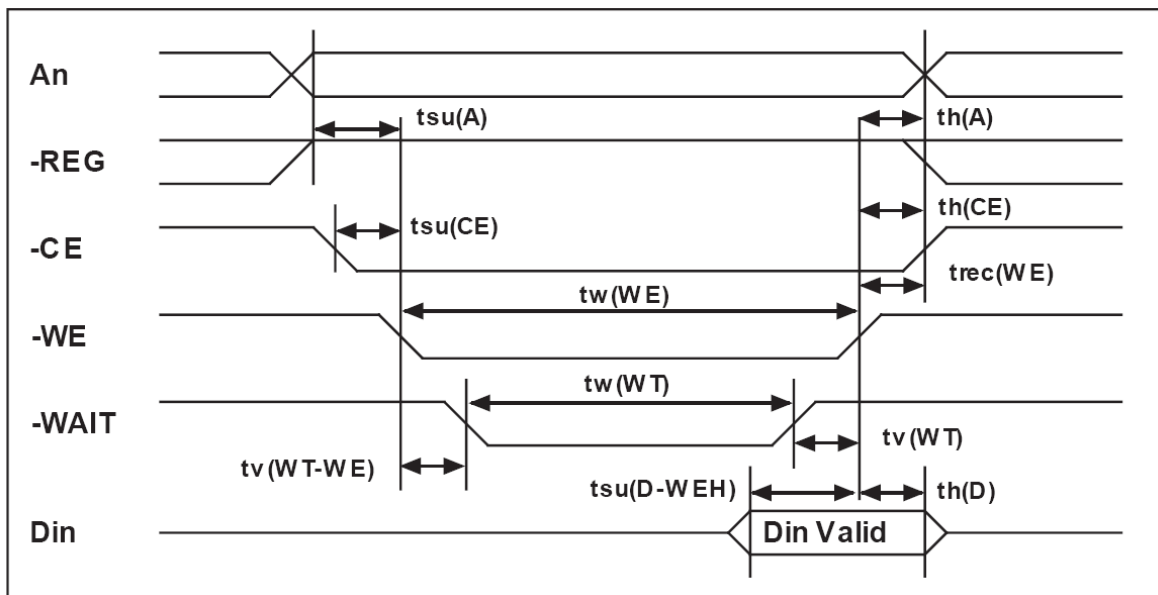
Figure 8: Common Memory Write Timing Diagram

4.6 I/O Input (Read) Timing

Table 23: I/O Read Timing

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item (unit: ns)	Symbol	IEEE Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold Following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD[3]	tdfINLACK(IORD)	tIGLIAL	0	45	0	na[1]	0	na[1]	0	na[1]
INPACK Delay Rising from IORD[3]	tdrINPACK(IORD)	tIGHIAH		45		na[1]		na[1]		na[1]
IOIS16 Delay Falling from Address[3]	tdfIOIS16	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IORD[3]	tdWT(IORD)	tIGLWTL		35		35		35		na[2]
Data Delay from Wait Rising[3]	td(WT)	tWTHQV		0		0		0		na[2]
Wait Width Time[3]	tw(WT)	tWTLWTH		350		350		350		na[2]

Notice:

1) –IOIS16 and –INPACK are not supported in this mode.

2) –WAIT is not supported in this mode.

3) Maximum load on –WAIT, -INPACK and –IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds.   Minimum time from –WAIT high to –IORD high is 0 nsec, but minimum –IORD width shall be met. Dout signifies data provided by the CompactFlash Storage Card to the system. Wait Width time meets PCMCIA specification of 12us but is intentionally less in this spec.
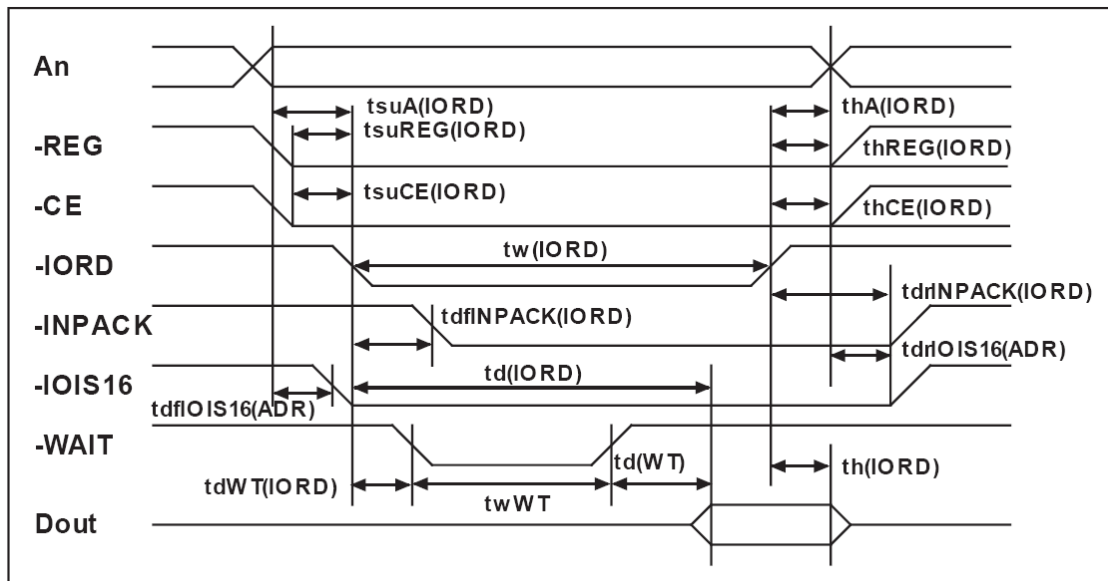
Figure 9: I/O Read Timing Diagram

4.7 I/O Input (Write) Timing

Table 24: I/O Write Timing

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item (unit: ns)	Symbol	IEEE Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold Following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling From Address[3]	tdfIOIS16(ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16(ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IOWR[3]	tdWT(IOWR)	tIWLWTL		35		35		35		na[2]
IOWR high from Wait high[3]	tdrIOWR(WT)	tWTJIWH	0		0		0		na[2]	
Wait Width Time[3]	tw(WT)	tWTLWTH		350		350		350		na[2]

Notice:

Notes:

1) –IOIS16 and –INPACK are not supported in this mode.

2) –WAIT is not supported in this mode.

3) Maximum load on –WAIT, -INPACK and –IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from –WAIT high to –IOWR high is 0 nsec, but minimum -IOWR width shall be met. Din signifies data provided by the system to the 12us but is intentionally less in this specification.
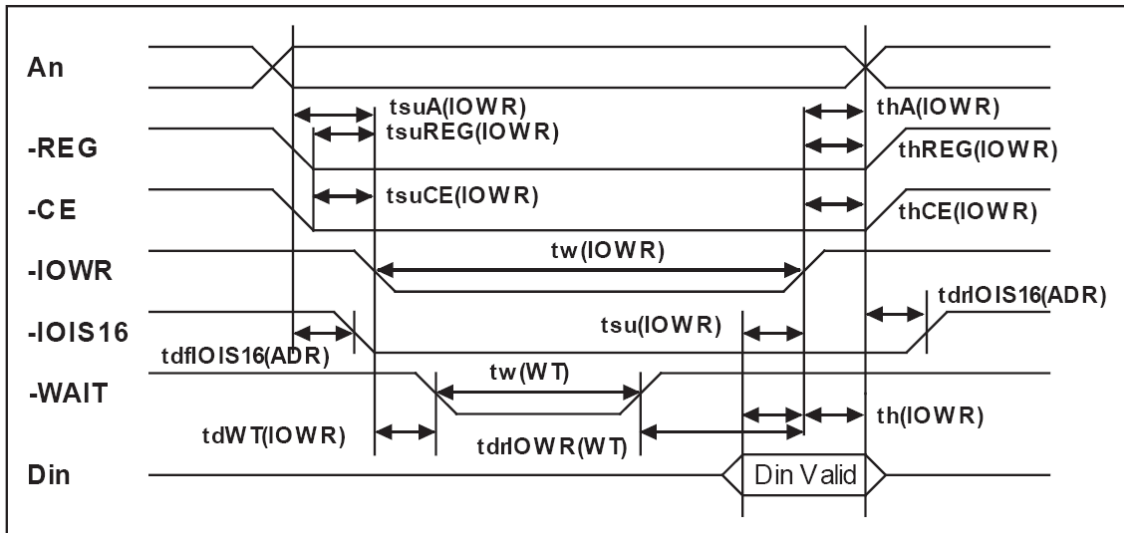
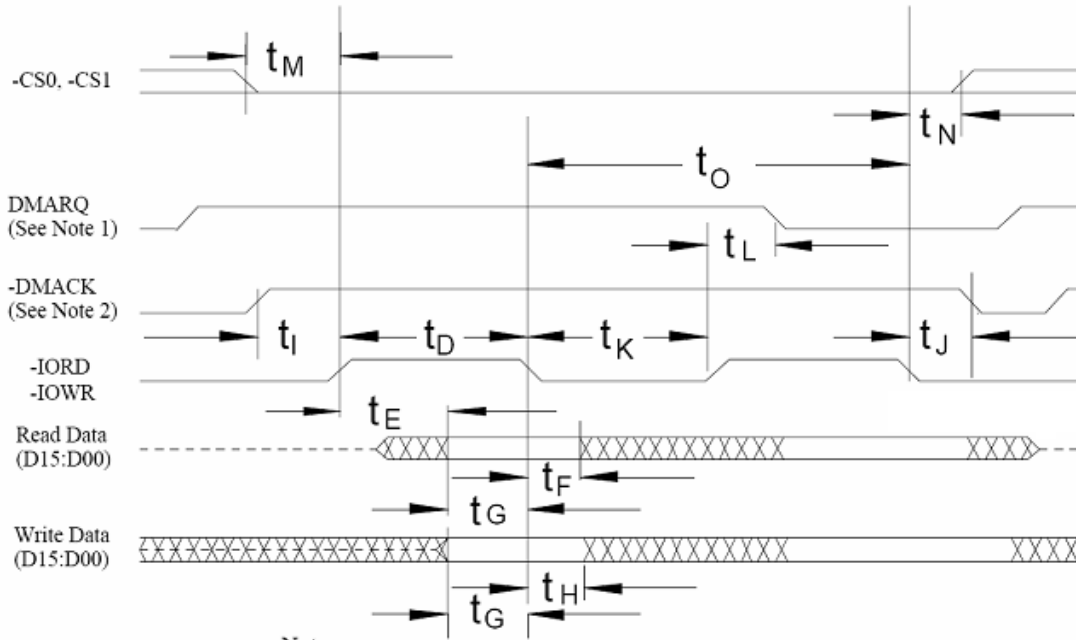**Figure 10: I/O Write Timing Diagram**

4.8 True IDE PIO Mode Read/Write Timing

The timing diagram for True IDE mode of operation in this section is drawn using the conventions in the ATA specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the –IORD, the –IOWR and the –IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Table 25: PIO Mode Read/Write Timing

	Item (unit: ns)	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
t_0	Cycle Time (min)[1]	600	383	240	180	120	100	80
t_1	Address Valid to –IORD/-IOWR setup (min)	70	50	30	30	25	15	10
t_2	-IORD/-IOWR(min) [1]	165	125	100	80	70	65	55
t_2	-IORD/-IOWR(min) Register (8bit) [1]	290	290	290	80	70	65	55
t_{2i}	-IORD/-IOWR recovery time(min) [1]	-	-	-	70	25	25	20
t_3	-IOWR data setup (min)	60	45	30	30	20	20	15
t_4	-IOWR data hold (min)	30	20	15	10	10	5	5
t_5	-IORD data setup(min)	50	35	20	20	20	15	10
t_6	-IORD data hold (min)	5	5	5	5	5	5	5
t_{6Z}	-IORD data tristate (max) [2]	30	30	30	30	30	20	20
t_7	Address valid to –IOCS16 assertion (max) [4]	90	50	40	na	na	na	na
t_8	Address valid to –IOCS16 released (max) [4]	60	45	30	na	na	na	na
t_9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10
t_{RD}	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0
t_A	IORDY Setup time[3]	35	35	35	35	35	na[5]	na[5]
t_B	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na[5]	na[5]
t_C	IORDY assertion to release(max)	5	5	5	5	5	na[5]	na[5]

Notice:

All timings are in nanoseconds. The maximum load on –IOCS16 is 1 LSTTL with a 50pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from –IORDY high to –IORD high is 0 nsec, but minimum –IORD width shall still be met.

- *t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time, The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. The Device implementation shall support any legal host implementation.*
- *This Parameter Specifies the time from the negation edge of –IORD to the time that the data bus is no longer driven by the Device (tri-state).*
- *The delay from the activation of –IORD or –IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the Device is not driving IORDY negated at tA after the activation of –IORD or –IOWR, then t5 shall be met and tRD is not applicable. If the Device is Driving IORDY negated at the time tA after the activation of –IORD or –IOWR, then tRD shall be met and t5 is not applicable.*
- *t7 and t8 apply only to modes0, 1 and 2. For other modes, this signal is not valid.*
- *IORDY is not supported in this mode.*
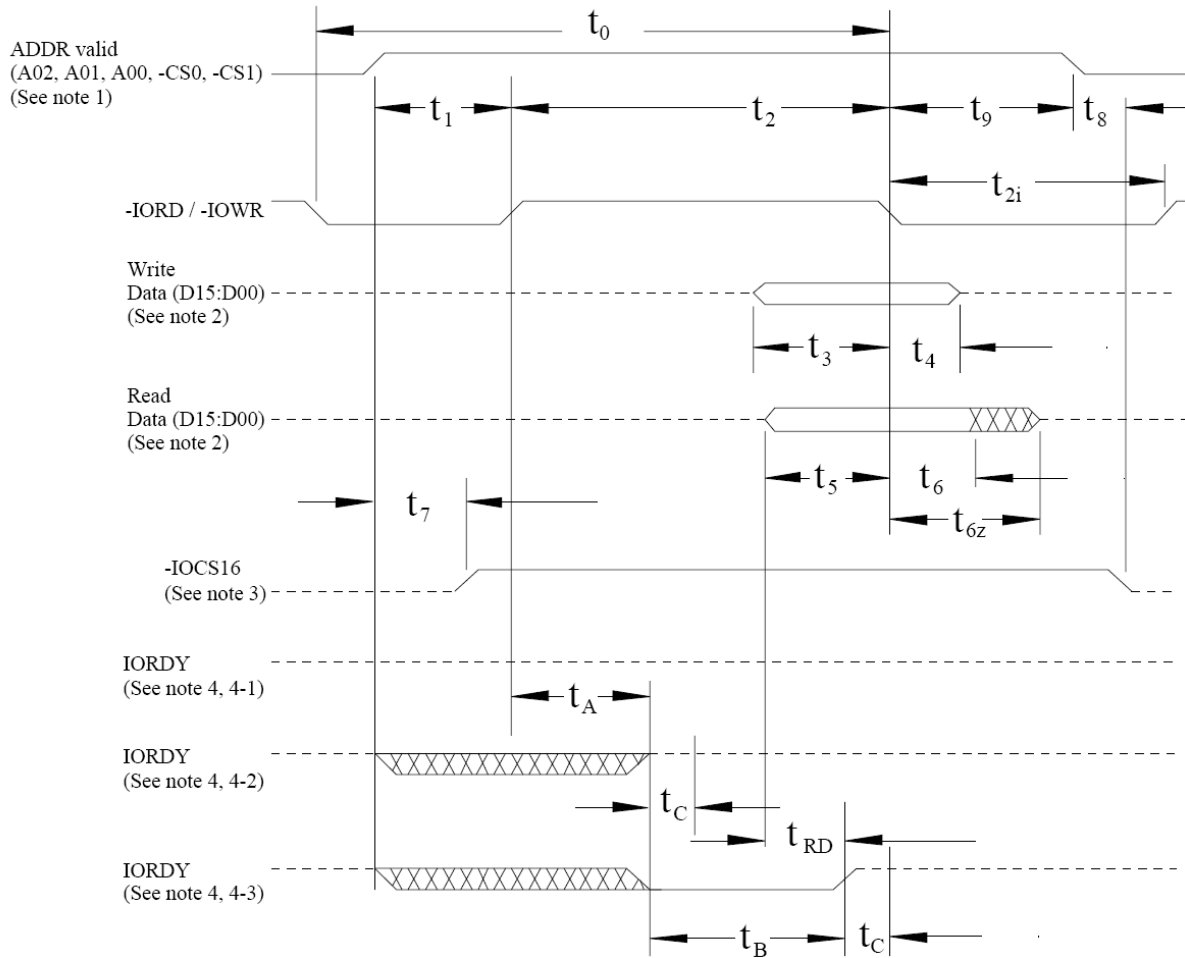
Notes:
(1) Device address consists of -CS0, -CS1, and A[02::00]
(2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
(3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
(4-1) Device never negates IORDY: No wait is generated.
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Figure 11: True IDE PIO Mode Timing Diagram

4.9 True IDE Multiword DMA Mode Read/Write Timing

The timing diagram for True IDE Multiword DMA mode of operation in this section is drawn using the conventions in the ATA specification. Signals are shown with their asserted sate as high regardless of whether the signal is actually negative or positive true. Consequently, the –IORD, the –IOWR and the –IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Table 26: Multiword DMA mode Read/Write Timing

	Item (Unit: ns)	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t_O	Cycle time (min)[1]	480	150	120	100	80
t_D	-IORD/ -IOWR asserted width (min)[1]	215	80	70	65	55
t_E	-IORD data access (max)	150	60	50	50	45
t_F	-IORD data hold(min)	5	5	5	5	5
t_G	-IORD/-IOWR data setup(min)	100	30	20	15	10
t_H	-IOWR data hold(min)	20	15	10	5	5
t_I	DMACK to –IORD/-IOWR setup (min)	0	0	0	0	0
t_J	-IORD/-IOWR to –DMACK hold (min)	20	5	5	5	5
t_{KR}	-IORD negated width (min)[1]	50	50	25	25	20
t_{KW}	-IOWR negated width (min)[1]	215	50	25	25	20
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	35	35
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35
t_M	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5
t_N	CS(1:0) hold	15	10	10	10	10

Notice:

1) t_O is the minimum total cycle time and t_D the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_O, t_D, t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW} for input and output cycles respectively. This mean a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_O is equal to or greater than the value reported in the device's identify device data. A device implementation shall support any legal host implementation.

Figure 12: True IDE Multiword DMA Read/Write Timing Diagram

4.10 True IDE Ultra DMA Mode Read/Write Timing

4.10.1 Ultra DMA Data Transfers Timing

Table 27 and Table 28 define the timings associated with all phases of Ultra DMA bursts.

Table 27: Ultra DMA Data Burst Timing Requirements

Item (Unit: ns)	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Measurement location[2]
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		Sender
t_{CYC}	112		73		54		39		25		[3]
t_{2CYC}	230		153		115		86		57		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		Host
t_{ZFS}	0		0		0		0		0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{FS}		230		200		170		130		120	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	[4]
t_{MLI}	20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10	[5]
t_{ZAG}	20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Host
t_{RFS}		75		70		60		60		60	Sender
t_{RP}	160		125		100		100		100		Recipient
t_{IORDYZ}		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		Sender

Notice:

1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5V.

2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and –DMARDY transitions are measured at the sender connector.

3) The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

4) The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5) The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turn around cycle.

6) See the AX Timing requirements in Table 30: Ultra DMA AC Signal Requirements.

<p style="text-align:center">**Table 28: Ultra DMA Data Burst Timing Descriptions**</p>

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until –DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from –DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing	
t_{DZFS}	Time from data output released-to driving until the first transition of critical timing	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAG}	Minimum delay time required for output	
t_{ZAD}	Drives to assert or negate (from released)	
t_{ENV}	Envelope time(from –DMACK to STOP and –HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time(no STROBE edges shall be sent this long after negation of –DMARDY)	
t_{RP}	Ready to pause time (that recipient shall wait to pause after negating –DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4
t_{ACK}	Setup and hold times for –DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notice:

1) The parameters t_{UI}, t_{MLI} (in Figure 16: Ultra DMA Data-In Burst Device Termination Timing and Figure 17: Ultra DMA Data-in Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

2) 80-condutor cabling shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 3) Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

4) For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

5) The parameters t_{DS} and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

Table 29: Ultra DMA Sender and Recipient IC Timing Requirements

Item (Unit: ns)	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DSIC}	14.7		9.7		6.8		6.8		4.8		
t_{DHIC}	4.8		4.8		4.8		4.8		4.8		
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5		
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0		
Ultra DMA Sender and Recipient IC Timing Description											
Name	**Comment**										
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note2)										
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)										
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)										
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)										

> **Notice:**
>
> 1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
>
> 2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V).
>
> 3) The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Table 30: Ultra DMA AC Signal Requirements

Name	Comment	Min[V/ns]	Max[V/ns]	Notes
S_{RISE}	Rising Edge Slew Rate for any signal		1.25	1
S_{FALL}	Falling Edge Slew Rate for any signal		1.25	1

> **Notice:**
>
> 1) The Sender shall be tested while driving an 18inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point in on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1pF, >100 Kohm, 1 GHz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

4.10.2 Initiating an Ultra DMA Data-In Burst

   a) An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 13: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Table 27: Ultra DMA Data Burst Timing Requirements and are described in Table 28: Ultra DMA Data Burst Timing Descriptions.

   b) The following steps shall occur in the order they are listed unless otherwise specifically allowed:

   c) The host shall keep –DMACK in the negated state before an Ultra DMA burst is initiated.

   d) The device shall assert DMARQ to initiate an Ultra DMA burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.

e) Steps(c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

f) The host shall negate –HDMARDY.

g) The host shall negate –CS0, -CS1, -DA2, -DA1, and DA0. The host shall keep –CS0, -CS1, DA2, DA1, and DA0 negated until after negating –DMACK at the end of the burst.

h) Steps(c), (d), and (e) shall have occurred at least tACK before the host asserts –DMACK. The host shall keep –DMACK asserted until the end of an Ultra DMA burst.

i) The host shall release D[15:00] within tAZ after asserting –DMACK.

j) The device may assert DSTROBE tZIORDY after the host has asserted -DMACK. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated -DMACK at the end of an Ultra DMA burst.

k) The host shall negate STOP and assert -HDMARDY within tENV after asserting -DMACK.

After negating STOP and asserting -HDMARDY, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).

l) The device shall drive D [15:00] no sooner than tZAD after the host has asserted -DMACK, negated STOP, and asserted -HDMARDY.

m) The device shall drive the first word of the data transfer onto D[15:00]. This step may occur when the device first drives D [15:00] in step (j).

n) To transfer the first word of data the device shall negate DSTROBE within tFS after the host has negated STOP and asserted -HDMARDY. The device shall negate DSTROBE no sooner than tDVS after driving the first word of data onto D [15:00].
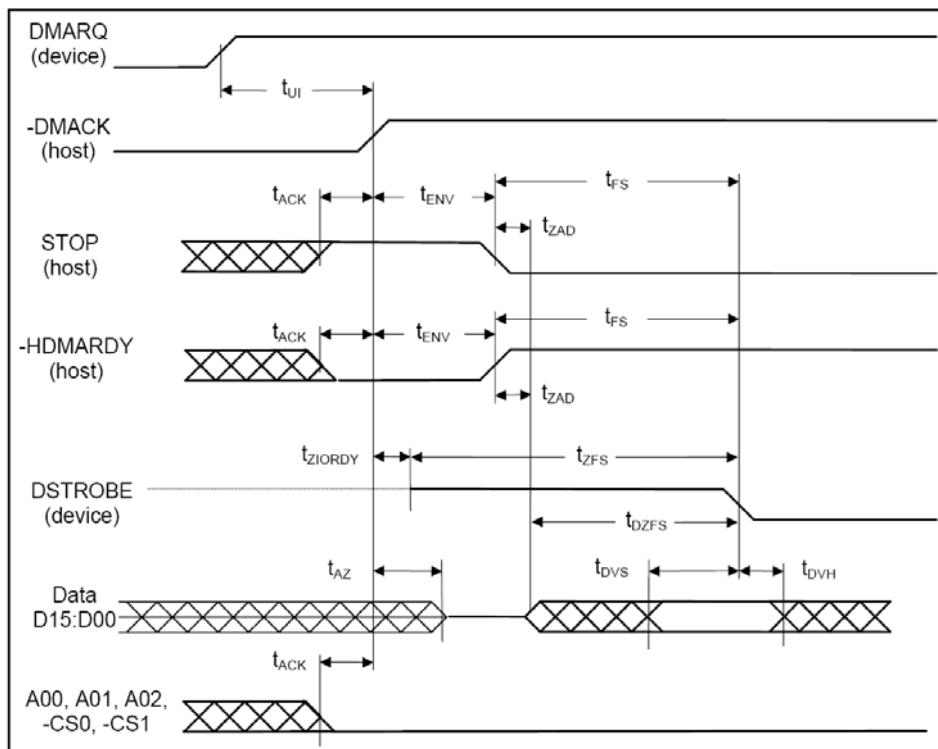
Figure 13: Ultra DMA Data-In Burst Initiation Timing

4.10.3 Sustaining an Ultra DMA data-In Burst

An Ultra DMA Data-In burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 14: Sustained Ultra DMA Data-In Burst Timing. The timing parameters are specified in Table 27: Ultra DMA Data Burst Timing Requirements and are described in Table 28: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall drive a data word onto D[15:00].

b) The device shall generate a DSTROBE edge to latch the new word no sooner than tDVS after changing the state of D [15:00]. The device shall generate a DSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.

c) The device shall not change the state of D[15:00] until at least tDVH after generating a DSTROBE edge to latch the data.

d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.
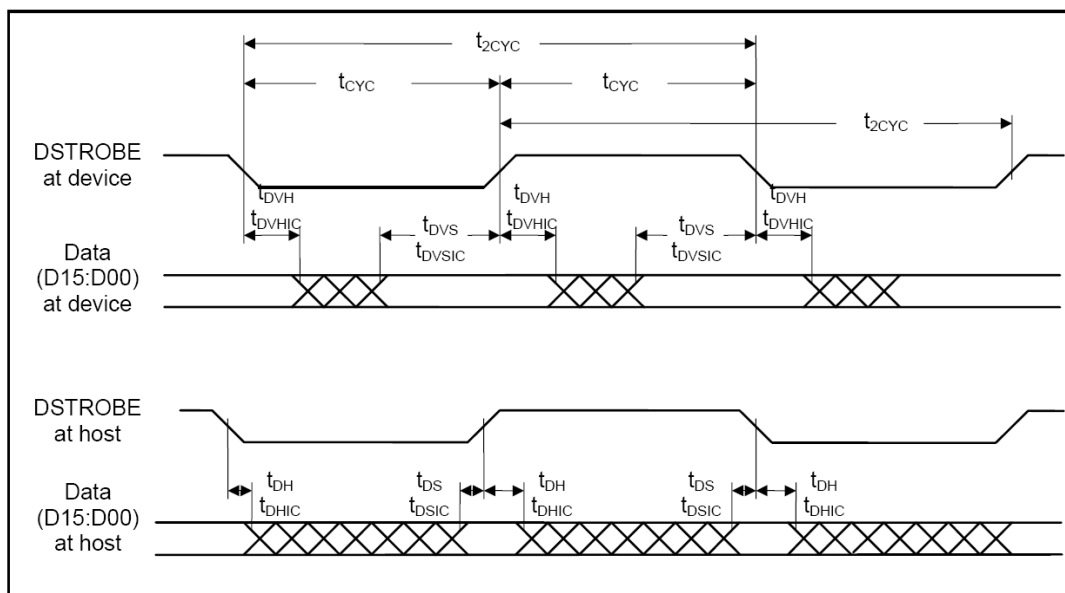
Notes: **D[15:00]** and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

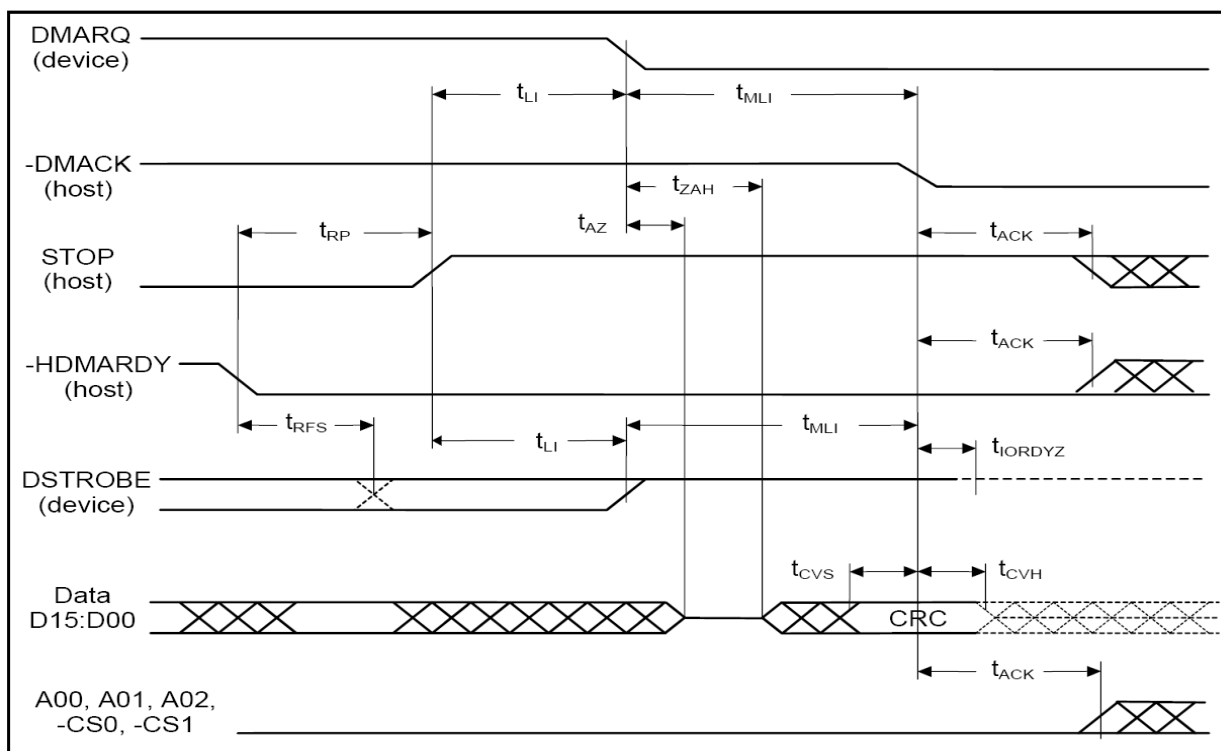**Figure 14: Sustained Ultra DMA Data-In Burst**

4.10.4 Host Pausing an Ultra DMA Data-In Burst

The host pauses a Data-In burst by following the steps lettered below. A timing diagram is shown in Figure 15: Ultra DMA Data-In Burst Host Pause Timing. The timing parameters are specified in Table 27: Ultra DMA Data Burst Timing Requirements and are described in Table 28: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b) The host shall pause an Ultra DMA burst by negating -HDMARDY.

c) The device shall stop generating DSTROBE edges within tRFS of the host negating -HDMARDY.

d) If the host negates -HDMARDY within tSR after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates -HDMARDY greater than tSR after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the device.

e) The host shall resume an Ultra DMA burst by asserting -HDMARDY.
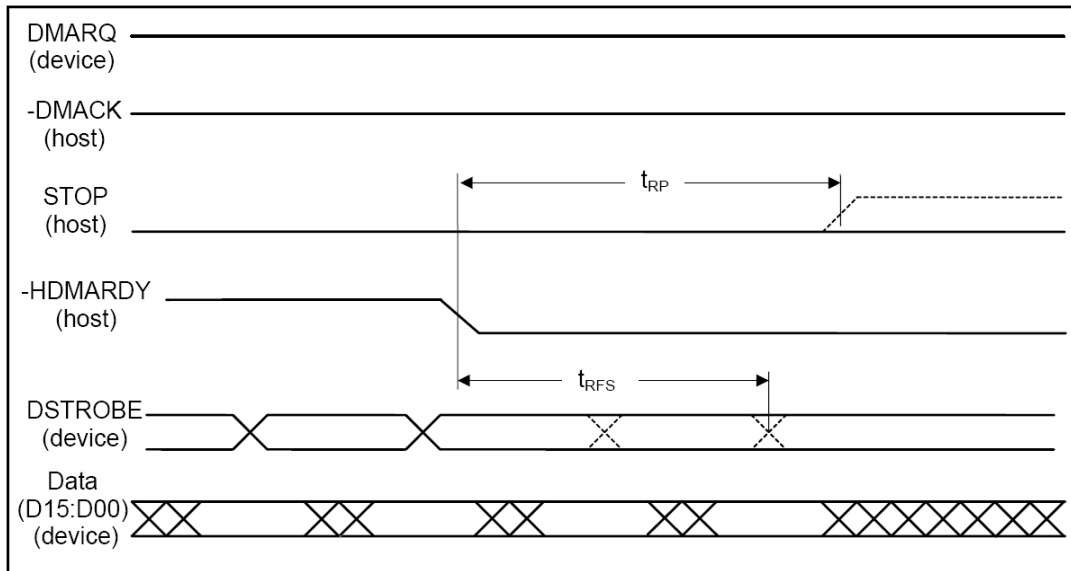
1) The host may assert STOP to request termination of the Ultra DMA burst no sooner than tRP after -HDMARDY is negated.

2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

Figure 15: Ultra DMA Data-In Burst Host Pause Timing

4.10.5 Device Terminating an Ultra DMA Data-In Burst

The device terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 16: Ultra DMA Data-In Burst Device Termination Timing. The timing parameters are specified in Table 27: Ultra DMA Data Burst Timing Requirements and are described in Table 28: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b) The device shall pause an Ultra DMA burst by not generating DSTROBE edges.

c) NOTE - The host shall not immediately assert STOP to initiate Ultra DMA burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate ULTRA DMA burst termination, the host shall negate -HDMARDY and wait t_{RP} before asserting STOP.

d) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.

Figure 16: Ultra DMA Data-In Burst Device Termination Timing

4.10.6 Host Terminating an Ultra DMA Data-In Burst

The host terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 17: Ultra DMA Data-In Burst Host Termination Timing. The timing parameters are specified in Table 27: Ultra DMA Data Burst Timing Requirements and are described in Table 28: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

b) The host shall initiate Ultra DMA burst termination by negating -HDMARDY. The host shall continue to negate -HDMARDY until the Ultra DMA burst is terminated.

c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating –HDMARDY.

d) If the host negates -HDMARDY within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDY greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

e) The host shall assert STOP no sooner than t_{RP} after negating -HDMARDY. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

f) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall

remain asserted until the Ultra DMA burst is terminated.

h) The device shall release D[15:00] no later than t_{AZ} after negating DMARQ.

i) The host shall drive DD D[15:00] no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive D[15:00] with the result of its CRC calculation.

j) If the host has not placed the result of its CRC calculation on D[15:00] since first driving D[15:00] during (9), the host shall place the result of its CRC calculation on D[15:00].

k) The host shall negate -DMACK no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated -HDMARDY, and no sooner than t_{DVS} after the host places the result of its CRC calculation on D[15:00].

l) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

m) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a mis-compare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred.

n) The device shall release DSTROBE within t_{IORDYZ} after the host negates -DMACK.

o) The host shall neither negate STOP nor assert -HDMARDY until at least t_{ACK} after the host has negated -DMACK.

p) The host shall not assert -IORD, -CS0, -CS1, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK

Notice: *The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated..*

Figure 17: Ultra DMA Data-In Burst Host Termination Timing
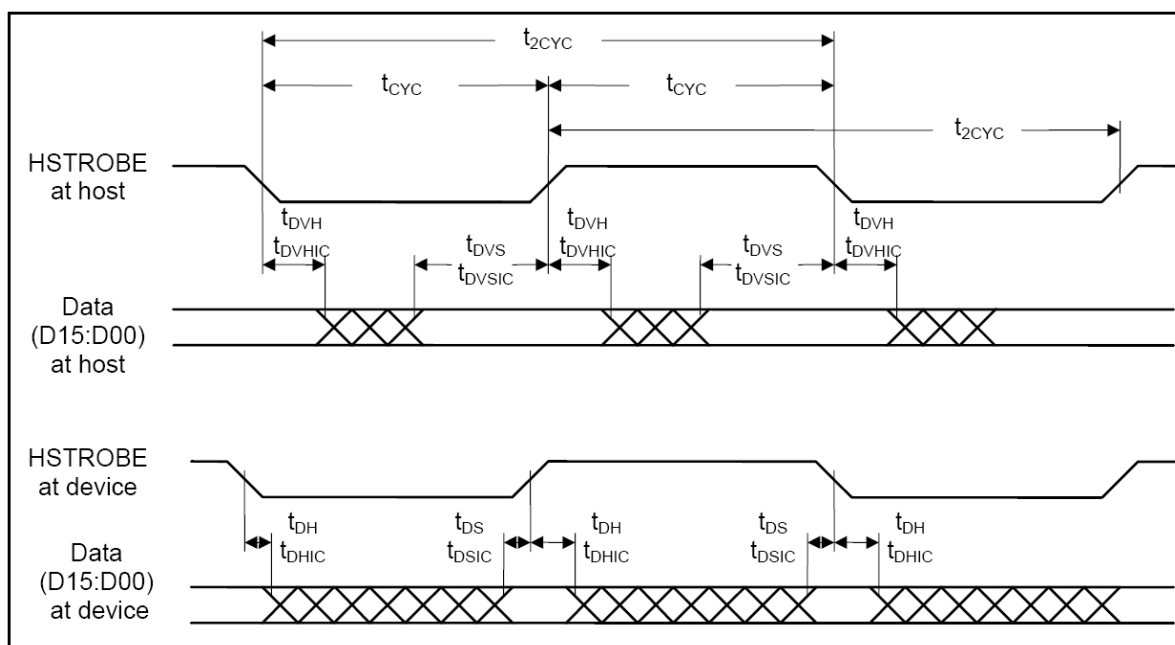
4.10.7 Initiating an Ultra DMA Data-Out Burst

An Ultra DMA Data-out burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 18: Ultra DMA Data-Out Burst Initiation Timing. The timing parameters are specified in Table 27: Ultra DMA Data Burst Timing Requirements and are described in Table 28: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.

b) The device shall assert DMARQ to initiate an Ultra DMA burst.

c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

d) The host shall assert HSTROBE.

e) The host shall negate -CS0, -CS1, DA2, DA1, and DA0. The host shall keep -CS0, -CS1, DA2, DA1, and DA0 negated until after negating -DMACK at the end of the burst.

f) Steps (c), (d), and (e) shall have occurred at least tACK before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA burst.

g) The device may negate -DDMARDY tZIORDY after the host has asserted -DMACK. Once the device has negated -DDMARDY, the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA burst.

h) The host shall negate STOP within tENV after asserting -DMACK. The host shall not assert STOP until after the first negation of HSTROBE.

i) The device shall assert -DDMARDY within tLI after the host has negated STOP. After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.

j) The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA burst initiation.

k) To transfer the first word of data: the host shall negate HSTROBE no sooner than tUI after the device has asserted -DDMARDY. The host shall negate HSTROBE no sooner than tDVS after the driving the first word of data onto D [15:00].
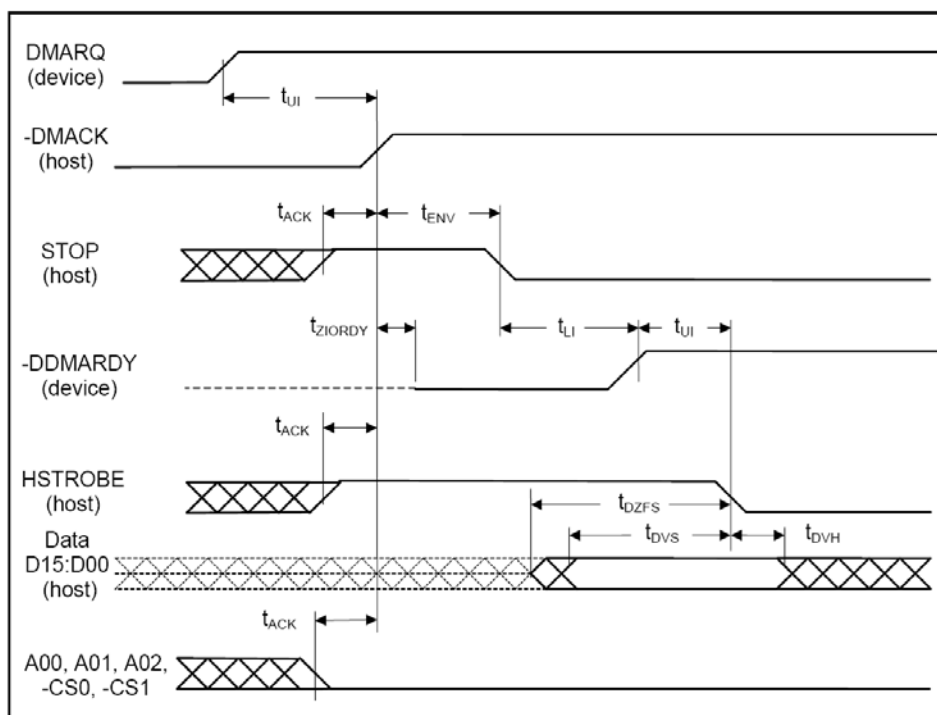
<u>*Notice:*</u> *The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.*
Figure 18: Ultra DMA Data-Out Burst Initiation Timing

4.10.8 Sustaining an Ultra DMA Data-Out Burst

An Ultra DMA Data-Out burst is sustained by following the steps lettered below. The timing diagram is shown in

Figure 19: Sustained Ultra DMA Data-Out Burst Timing. The associated timing parameters are specified in Table 27: Ultra DMA Data Burst Timing Requirements and are described in Table 28: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall drive a data word onto D [15:00].

b) The host shall generate an HSTROBE edge to latch the new word no sooner than tDVS after changing the state of D [15:00]. The host shall generate an HSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.

c) The host shall not change the state of D[15:00] until at least tDVH after generating an HSTROBE edge to latch the data.

d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

Notice: *Data (D15:D00) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.*

Figure 19: Sustained Ultra DMA Data-Out Burst Timing

4.10.9 Device Pausing an Ultra DMA Data-Out Burst

The device pauses an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram is shown in Figure 20: Ultra DMA Data-Out Burst Device Pause Timing. The timing parameters are specified in Table 27: Ultra DMA Data Burst Timing Requirements and are described in Table 28: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b) The device shall pause an Ultra DMA burst by negating -DDMARDY.

c) The host shall stop generating HSTROBE edges within tRFS of the device negating -DDMARDY.

d) If the device negates -DDMARDY within tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or

two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the host.

e) The device shall resume an Ultra DMA burst by asserting -DDMARDY.

Figure 20: Ultra DMA Data-Out Burst Device Pause Timing
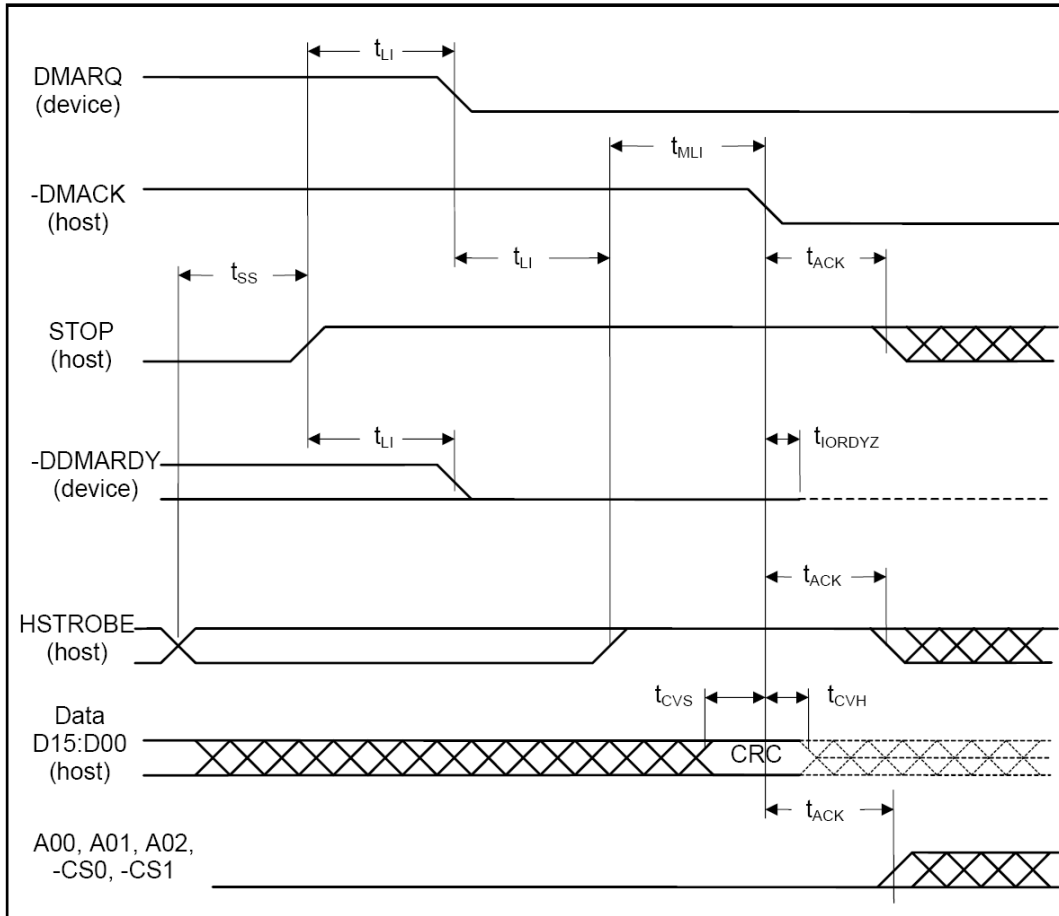
4.10.10 Device Terminating an Ultra DMA Data-Out Burst

The device terminates an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram for the operation is shown in Figure 21: Ultra DMA Data-Out Burst Device Termination Timing. The timing parameters are specified in Table 27: Ultra DMA Data Burst Timing Requirements and are described in Table 28: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

b) The device shall initiate Ultra DMA burst termination by negating -DDMARDY.

c) The host shall stop generating an HSTROBE edges within tRFS of the device negating -DDMARDY.

d) If the device negates -DDMARDY within tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the host.

e) The device shall negate DMARQ no sooner than tRP after negating -DDMARDY. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

f) The host shall assert STOP within tLI after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

g) If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE

shall remain asserted until the Ultra DMA burst is terminated.

h) The host shall place the result of its CRC calculation on D[15:00]

i) The host shall negate -DMACK no sooner than tMLI after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than tDVS after placing the result of its CRC calculation on D[15:00].

j) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

k) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a mis-compare error occurs during one or more Ultra DMA bursts for any one command,

Figure 21: Ultra DMA Data-Out Burst Device Termination Timing

4.10.11 Host Terminating an Ultra DMA Data-Out Burst

Termination of an Ultra DMA Data-Out burst by the host is shown in Figure 22: Ultra DMA Data-Out Burst Host Termination Timing while timing parameters are specified in Table 27: Ultra DMA Data Burst Timing Requirements and timing parameters are described in Table 28: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.

b) The host shall assert STOP no sooner than tSS after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

c) The device shall negate DMARQ within tLI after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

d) The device shall negate -DDMARDY within tLI after the host has negated STOP. The device shall not assert -DDMARDY again until after the Ultra DMA burst termination is complete.

e) If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.

f) The host shall place the result of its CRC calculation on D[15:00].

g) The host shall negate -DMACK no sooner than tMLI after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than tDVS after placing the result of its CRC calculation on D[15:00].

h) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

i) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a mis-compare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.

j) The device shall release -DDMARDY within t IORDYZ after the host has negated -DMACK.

k) The host shall neither negate STOP nor negate HSTROBE until at least tACK after negating -DMACK.

l) The host shall not assert -IOWR, -CS0, -CS1, DA2, DA1, or DA0 until at least tACK after negating -DMACK.
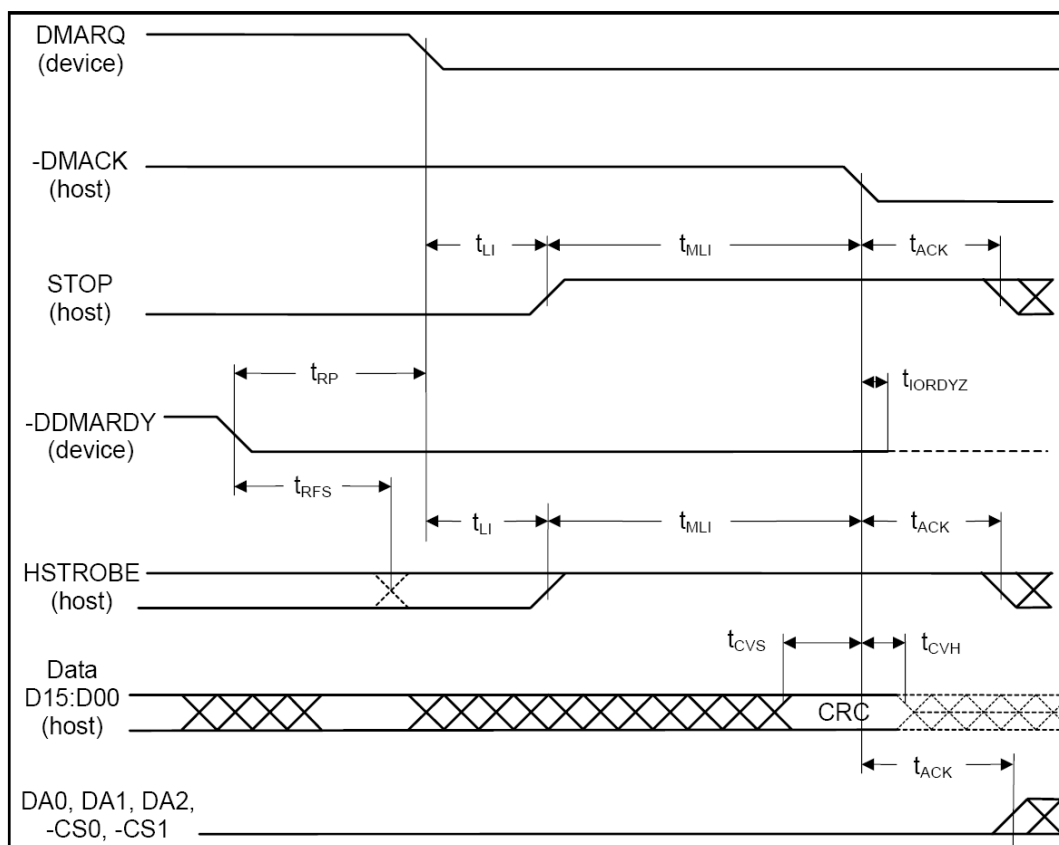
**Figure 22: Ultra DMA Data-Out Burst Host Termination Timing**

5. Installation

5.1 Installation

- For Installation of DiskOnModule to your system, please follow up below steps;

    1. Make sure your computer is turned off before you open the case.

    2. Plug the DiskOnModule carefully into the IDE slot on your computer or host adapter.

    3. Connect the power cable of the DiskOnModule.

    4. Check cable connections and DiskOnModuel is firm enough.

5.2 Partition

- For DOS Operating System：

    1. Get into your windows system. You can Click the 『Start』→『Control Panel』→『Administrative Tools』→ 『Computer Management』 then select 『Storage』→『Disk Manager』 to setup the partition.
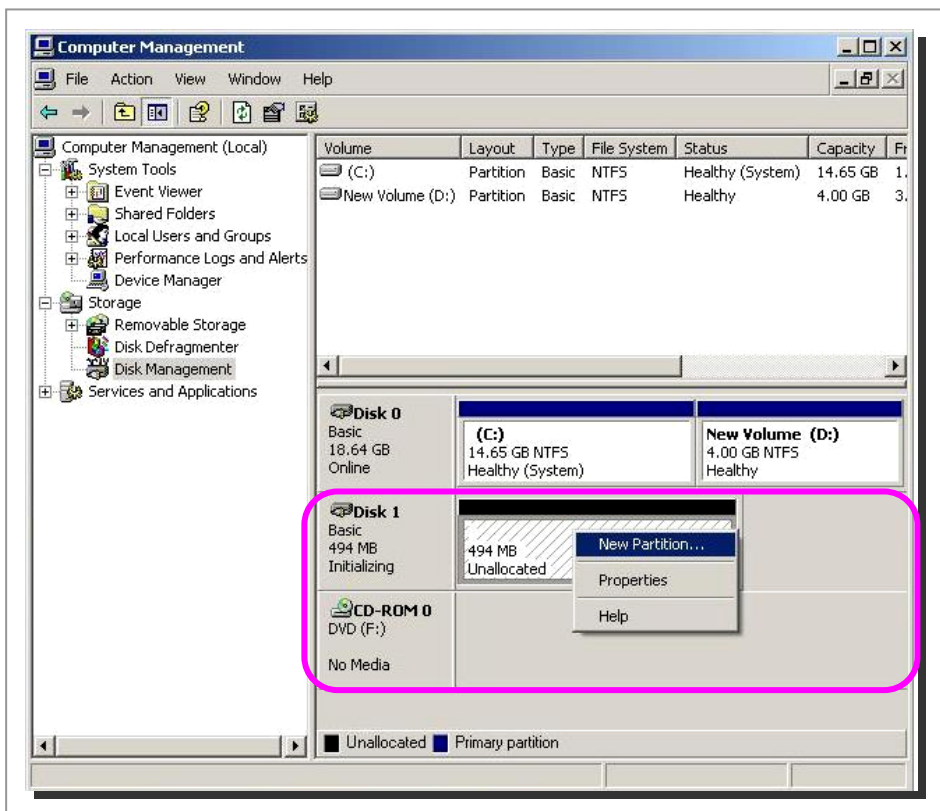
5.3 Format

- For DOS Operating System：

    - Before you format or partition your new DiskOnModule, you must configure your computer's BIOS so that the computer can recognize your new DiskOnModule.

    1. Turn your computer on. As your computer start up, watch the screen for a message describing how to run the system setup program (sometimes called BIOS or CMOS setup). This is usually done by pressing a special key, such as DELETE, ESC, or F1, during startup. See your computer manual for details. Press the appropriate key to run the system setup program.

    2. If your BIOS provides automatic drive detection (an "AUTO" drive type), select this option. (If you use

Normal/CHS mode to partition your DOM, you can get the maximum formatted capacity.)

This allows your computer to configure itself automatically for your new DiskOnModule.

If your BIOS does not provide automatic drive detection, select "User-defined" drive setting and enter the CHS values from the table.

BIOS Settings (see specification)

Capacity   Cylinders   Heads   Sectors   (unformatted)

3. Save the settings and exit the System Setup program.

(Your computer will be automatically rebooted.)

● For Windows Operating System：

- To partition your new DOM, for example use Microsoft WindowsXP and WindowsXP embedded system：

1. Click the 『Start』→『Control Panel』→『Administrative Tools』→『Computer Management』 then select 『Storage』→『Disk Manager』 to setup the file format.

2. Select "FAT or NTFS" format for user.
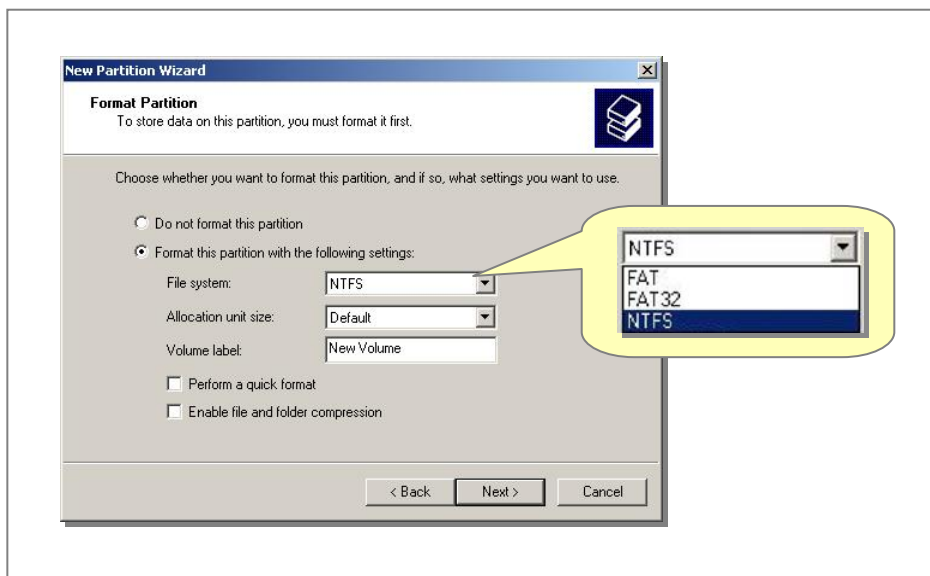
6. Troubleshooting

6.1 BIOS can not identify DiskOnModule

a. Check Power Cable Status

b. Check Connector status

c. Check the Power Voltage (5V or 3.3V)

6.2 DOM can not boot the system

a. Check BIOS setting

b. Reinstall your system

Notice : *Please contact your closest CSS or PQI office for verifying your other troubles.*

7. Ordering Information

HAK40	-	128M	R	01	0	0	00
|	|	|	|	|	|	|	|
Series	Range	Size	Green	Outline	Alternative	Level	Option

Table 31: HAK40 Ordering Information

Code	Definition	Description
HAK40	Series name	Product Series name, fixed
-	Temperature range	"-": Industrial, "W": Wide temperature
128M	Memory size	128M: 128MB, 256M: 256MB, 512M: 512MB, 001G: 1GB, 002G: 2GB, 004G: 4GB, 008G: 8GB, 016G: 16GB
R	Green level	"R": RoHS/PFOS
01	Device outline	First digit is reserved as "0". Second digit defines performance and switch options. Please see the data sheet or contact CSS or PQI for details.
0	Alternative	Reserved
0	Level	Reserved
00	Option	Option for customization

8. Contact Information

CoreSolid Storage Corporation, a TDK-PQI storage business company, specializes in the design and marketing of SSD, DOM, and Industry CF products.

For further information, please reach us at the following contact information:

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